# A Prediction Method of Heat Generation in the Silicon Substrate for 3-D ICs

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***Abstract*—Through-silicon via (TSV) based 3-D ICs provide a promising solution for miniaturizing chips. However, thermal issue in 3-D ICs cannot be ignored. In this paper, we proposed a method based on 3-D transmission line matrix (3-D TLM) method to calculate heat generation in the lossy silicon substrate caused by TSV induced electrical field. Pseudo random bit sequences (PRBS) at different bit rates are fed into TSVs to simulate the transmitted digital signal. The influence of TSV arrangements and TSV oxide thickness to the heat generation are also investigated in time-domain. With the help of this method, the generation and distribution of heat in the silicon substrate can be predicted.**

***Keywords—3-D IC, Through-silicon via (TSV), silicon substrate noise, heat generation***

## I. INTRODUCTION

To raise the performance of electronic devices, the methods to realize chips of higher data rate and less area are being studied. Three-dimensional integrated circuits (3-D ICs) have been one of the most promising technologies, thus viewed as the solution to break the physical limit predicted by Moore's law. Through-silicon vias (TSVs) are the key components in 3-D ICs which provide a shorter path and wider bandwidth of data transmission by enabling vertical connection between different IC layers. But on the other hand, some problems also encountered in 3-D ICs such as thermal issue because the multilayer structures obstruct the paths of heat conduction [1].

Except for the sources of heat generation in traditional ICs such as switching transistors and metal traces that transmit signal, in 3-D ICs, currents may also leak into the lossy silicon substrate through the capacitive isolation layer of TSVs. Leakage current not only causes signal integrity issues of TSVs, but also leads to additional heat generation in the substrate which is more crucial than heat produced on traces because of the high thermal resistance of silicon. This heat source is seldom considered in the conventional researches, but cannot be ignorable in the wide I/O structure which requires high-density TSV array and high data transmit rates.

In this paper, a prediction method for heat generation in the silicon substrate is proposed based on three-dimensional transmission-line matrix (3-D TLM) method. By segmenting the TSVs and silicon substrate into numerous cells, the detail of heat sources can be achieved. In addition, with this method, the effect of the data rate, arrangement of TSVs, oxide thickness to the heat generation can also be obtained.

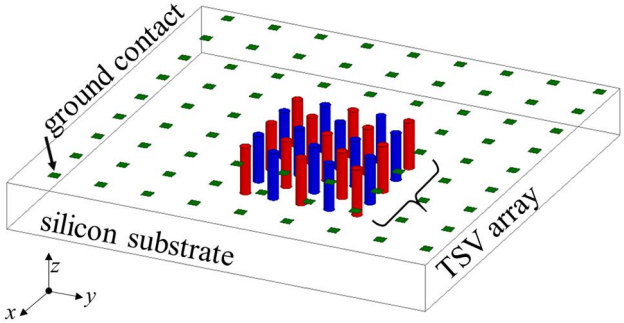


Fig. 1. A scenario of TSV-based 3-D IC, including a silicon substrate, TSV array inside the substrate, and ground contacts on the surface of the substrate. Red circles are source TSVs and blue one are ground TSVs.

## II. PROPOSED METHOD

### A. 3-D Transmission Line Matrix Method

Fig. 1 shows a typical structure of TSV-based 3-D ICs where TSV arrays consisting of metal pillars surrounded by oxide (or other insulator) are placed inside the silicon substrate. The TSV array is checkered with signal and ground TSVs for better signal integrity. Ground contacts are formed on the top surface of silicon substrate to provide correct bias and to isolate the noise in the substrate. The physical parameters of the structure are listed in Table I. To obtain the detail information of voltage distribution in the substrate, 3-D TLM method was proposed in [2]. As illustrated in Fig. 2, the TSVs and silicon substrate are both segmented into cells. A substrate cell is composed of 6 pairs of resistors and capacitors in 6 directions of a cubic, and each RC pair models the current flowing through the surface of that direction. Silicon substrate with different doping profile will have distinct resistivity, which could be modeled with the resistors in a substrate cell.

As to TSVs, an axisymmetric cell is used to represent the cylinder aperture. In a TSV cell, 4 identical capacitors are placed in *x*-*y* plane to model the insulating oxide layer. This insulating capacitor is a key factor to isolate the signal on TSVs from the lossy silicon substrate and could be easily derived from cylindrical capacitance formula. In the *z* direction, a resistor and an inductor in series are employed to model the metal core of the TSV, and mutual inductors are utilized to model the coupling between TSVs.

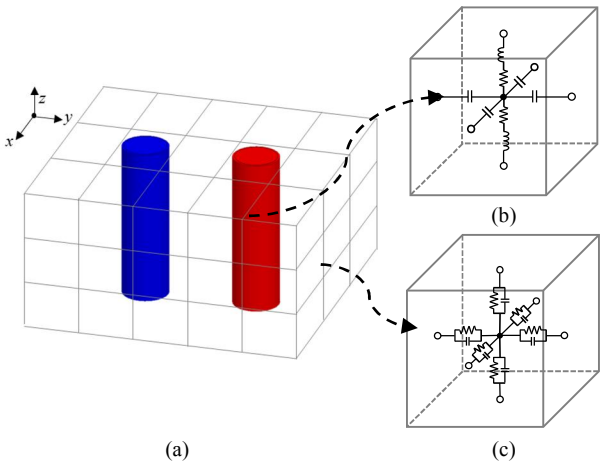


Fig. 2. 3-D TLM method applied to the silicon substrate with TSVs. (a) Part of the structure to be modeled. (b) Cell of TSV. (c) Cell of silicon substrate.

TABLE I
PARAMETERS OF THE STRUCTURE TO BE MODELED

| **Parameter** | **Value** |
|---|---|
| Length of TSVs | 50 μm |
| Diameter of TSVs | 10 μm |
| Pitch of TSVs | 30 μm |
| Thickness of oxide layer | 0.5 μm |
| Resistivity of silicon substrate | 10 Ω-cm |
| Size of silicon substrate | 450 x 450 $\mu m^2$ |
| Size of ground contacts | 10 x 10 $\mu m^2$ |
| Pitch of ground contacts | 50 μm |
| Cell size | 10 x 10 x 10 $\mu m^3$ |

### B. *Derive Voltage Distribution in the Substrate*

Once the 3-D TLM model is constructed, S-parameters and eye diagrams could be obtained using circuit simulation tools [3]. On top of that, the voltage level of each node in all the substrate cells can be calculated and plotted with MATLAB [4]. Sinusoidal voltage sources with frequency of 1 GHz and voltage level of 1.2 V are excited at one side of the source TSVs in Fig. 1, while TSV array on the other side are all terminated with 50 Ω resistances. The voltage distribution on the top surface of the substrate ($z$ = 50 μm) when input signal reaches its maximum is plotted in Fig. 3. The red and blue circles at the center stand for signal and ground TSVs, respectively. The blue squares at the outer region of the substrate indicating the ground contacts. When transmitting signals, a portion of the signal leaks into the substrate and causes substrate noise. Large substrate noise may lead to failure of active circuits, which is known as signal integrity problem. Hence, there should be no active circuits placed near TSVs. In addition, the noise will be transformed to heat when flowing in the lossy silicon substrate, which will also cause thermal problem. To calculate how much heat generated in the silicon substrate, voltage distribution given from 3-D TLM could be utilized. For a substrate cell, the time-average dissipated power (and corresponding to heat generation) can be calculated by

$$\langle P_{dis} \rangle = \frac{1}{T}\int_t \left( \sum_{i=1}^{6} \frac{(V_i - V_c)^2}{R_{Si}} \right) dt \quad , \tag{0}$$

where $R_{si}$ is the resistance in the substrate cell, $V_c$ is the voltage at the center of the substrate cell, $V_i$ is the voltage at each surface node of the substrate cell, and $T$ is the total simulation time.

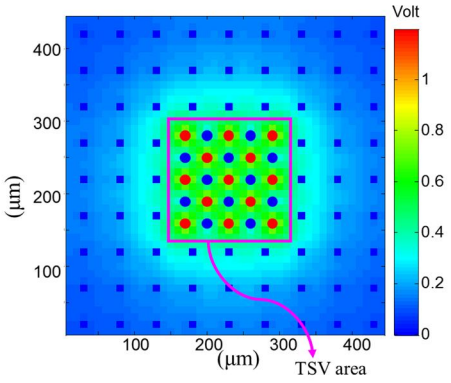


Fig. 3. Voltage distribution on the top surface of the silicon substrate.

## III. SIMULATION RESULTS AND DISSCUSION

### A. *Heat Generation Distribution*

To model the wide I/O memory applications, the signal sources are changed to pseudo random bit sequences (PRBS) at different bit rates. With (1), the time-average generated heat in each substrate cell can be calculated. Summing up the heat power along the $z$-direction, the 2-D plot of heat generation is illustrated in Fig. 4. It could be recognized that most of the heat are generated near TSVs, where the electric field is strong. In the area of interest, as marked with purple line and labeled with ***TSV area*** in Fig. 3, the generated heat is about 96.8% of the total dissipated power. This indicates that the heat generation at outer part of substrate is small enough to be ignored.

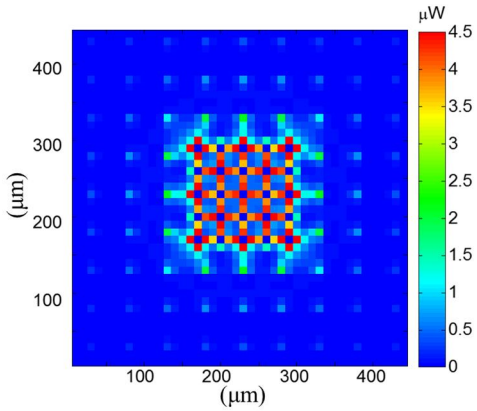


Fig. 4. Plot of 2-D heat generation, where the power has been summed along $z$ direction.

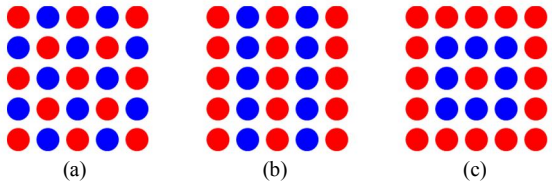


Fig. 5. Different arrangement of TSVs. The red circles represent signal TSVs and the blue ones are ground TSVs. (a) Checkered arrangement. (b) Aligned arrangement. (c) Concentric arrangement.

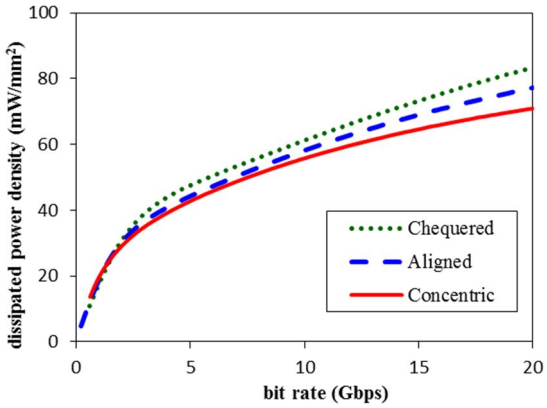


Fig. 6. Time-average power density (normalized to TSV area) for different types of arrangements.

### B. *Influence of TSV Arrangement*

Fig. 5 shows three different types of TSV layouts including checkered, aligned, and concentric arrangements. In checkered arrangement, each signal TSV is surrounded with 4 ground TSVs and vice versa. In aligned one, the TSVs with the same characteristic (signal or ground) are placed in row, and ground rows are adjacent to the signal rows. As to the concentric one, signal and ground TSVs are arranged in concentric squares. All of these structures are simulated with 3-D TLM method in which signal TSVs are excited with PRBS to observe how the arrangement of TSV array influence the heat generation in the substrate. Fig. 6 shows the simulated time-average dissipated power density which is normalized to the TSV area. At low data rate, it is obvious that the generated heat is almost the same for all the three cases. But as the bit rate comes to 20 Gbps, the heat generated by concentric arrangement is only 80% of checkered one, even though there are more signal TSVs in the concentric case. This indicates that it will be a trade-off between crosstalk level (which is lowest in checkered arrangement) and heat generation in silicon substrate.

### C. *Influence of Oxide Thickness*

The insulating oxide thickness is a crucial parameter for determining substrate noise. Thicker oxide could provide better isolation between TSVs and the substrate, resulting in less power dissipation in the substrate. Fig. 7 demonstrates how power dissipation varies with PRBS bit rates in different oxide thickness, and the dissipated power density difference between 0.2 μm and 1.0 μm oxide can be as high as 170% at 20 Gbps. Although widening oxide thickness is an effective way to reduce heat generation and crosstalk at the same time, maximum oxide thickness is limited by the TSV manufacturing process. With this method, the heat from substrate can be easily counted into thermal budget when designing.

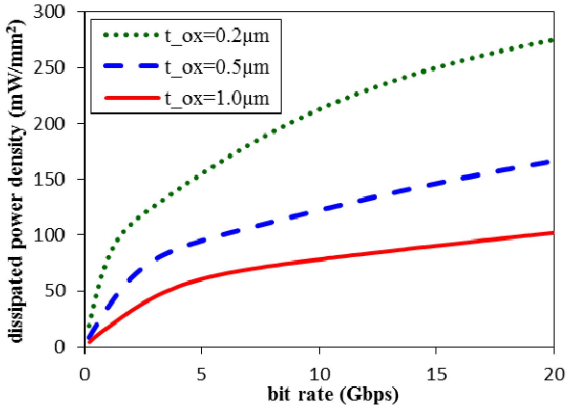


Fig. 7. Time-average power density (normalized to TSV area) for different oxide thickness.

## IV. Conclusion

In this paper, 3-D TLM method is utilized to determine heat generation in the lossy silicon substrate as signal transmitted through TSVs. Heat generation distribution in x-y plane shows the power is mostly generated near the TSV array. Total dissipated power density is compared under different scenarios, including various oxide thickness and TSV arrangements. The result shows that the concentric arrangement causes less heat generation while having most signal TSVs, and thicker insulating oxide thickness decisively reduces the heat generated in the silicon substrate.

## Acknowledgment

This research is partially supported by the Ministry of Science and Technology in Taiwan under Grant no. MOST 103-2218-E-002 -003 -.

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