Transmission Line Basics

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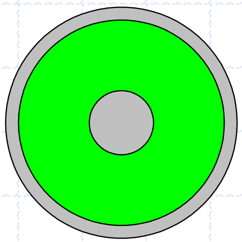
Outlines

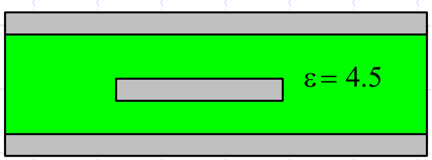
- Transmission Lines in Planar structure.
- Key Parameters for Transmission Lines.
- Transmission Line Equations.
- Analysis Approach for Z_0 and T_d
- Intuitive concept to determine Z_0 and T_d
- Loss of Transmission Lines
- Example: Rambus and RIMM Module design

Transmission Lines in Planar structure

Homogeneous

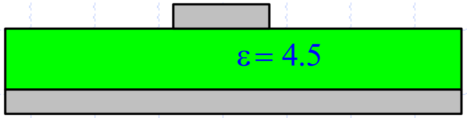


Coaxial Cable

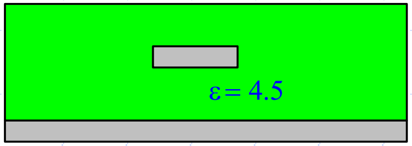


Stripline

Inhomogeneous



Microstrip line



Embedded Microstrip line

Key Parameters for Transmission Lines

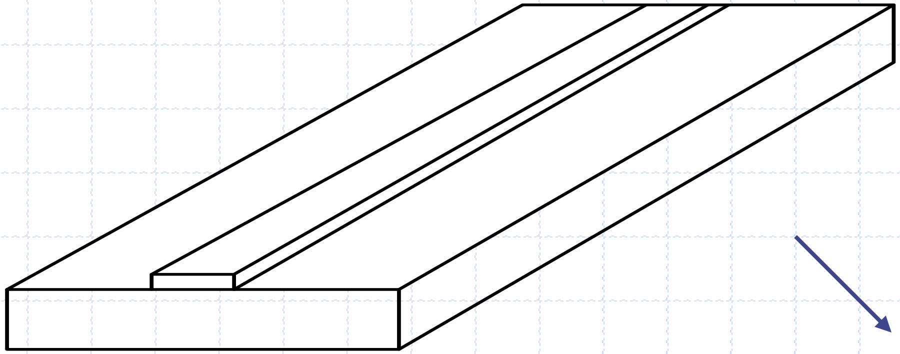
1. Relation of V / I : Characteristic Impedance Z_0
2. Velocity of Signal: Effective dielectric constant ε_e
3. Attenuation: Conductor loss α_c

   Dielectric loss α_d

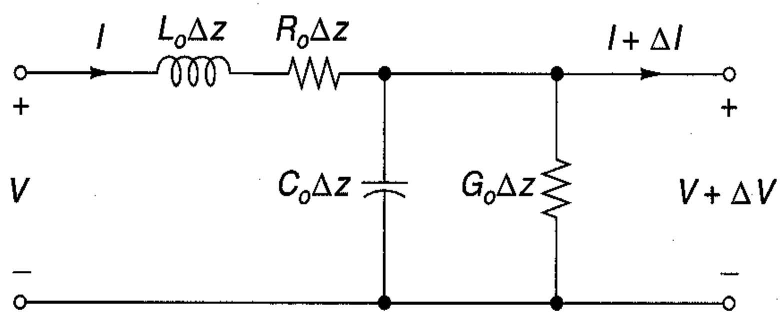
Lossless case

Z_0	$\sqrt{\frac{L}{C}}$	$\frac{1}{V_p C}$	$\frac{T_d}{C}$
V_p	$\frac{1}{\sqrt{LC}}$	$\frac{c_0}{\sqrt{\varepsilon_e}}$	$\frac{1}{T_d}$

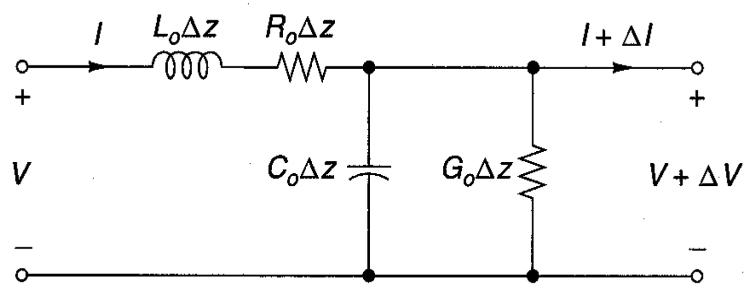
Transmission Line Equations



Quasi-TEM assumption



Transmission Line Equations



R_0 = resistance per unit length(Ohm / cm)

G_0 = conductance per unit length (mOhm / cm)

L_0 = inductance per unit length (H / cm)

C_0 = capacitance per unit length (F / cm)

KVL : $$\frac{dV}{dz} = -(R_0 + jwL_0)I$$

KCL : $$\frac{dI}{dz} = -(G_0 + jwC_0)V$$

→ Solve 2nd order D.E. for V and I

Transmission Line Equations

Two wave components with amplitudes
V+ and V- traveling in the direction of +z and -z

$$V = V_+ e^{-rz} + V_- e^{+rz}$$

$$I = \frac{1}{Z_0}(V_+ e^{-rz} - V_- e^{+rz}) = I_+ + I_-$$

Where propagation constant and characteristic impedance are

$$r = \sqrt{(R_0 + jwL_0)(G_0 + jwC_0)} = \alpha + j\beta$$

$$Z_0 = \frac{V_+}{I_+} = \frac{V_-}{I_-} = \sqrt{\frac{R_0 + jwL_0}{G_0 + jwC_0}}$$

Transmission Line Equations

α and β can be expressed in terms of (R_0, L_0, G_0, C_0)

$$\alpha^2 - \beta^2 = R_0 G_0 - \omega^2 L_0 C_0$$

$$2\alpha\beta = \omega(R_0 C_0 + G_0 L_0)$$

The actual voltage and current on transmission line:

$$V(z,t) = \mathrm{Re}[(V_+ e^{-\alpha z} e^{-j\beta z} + V_- e^{+\alpha z} e^{j\beta z}) e^{jwt}]$$

$$I(z,t) = \mathrm{Re}[\frac{1}{Z_0}(V_+ e^{-\alpha z} e^{-j\beta z} - V_- e^{+\alpha z} e^{j\beta z}) e^{jwt}]$$

Analysis approach for Z_0 and T_d (Wires in air)

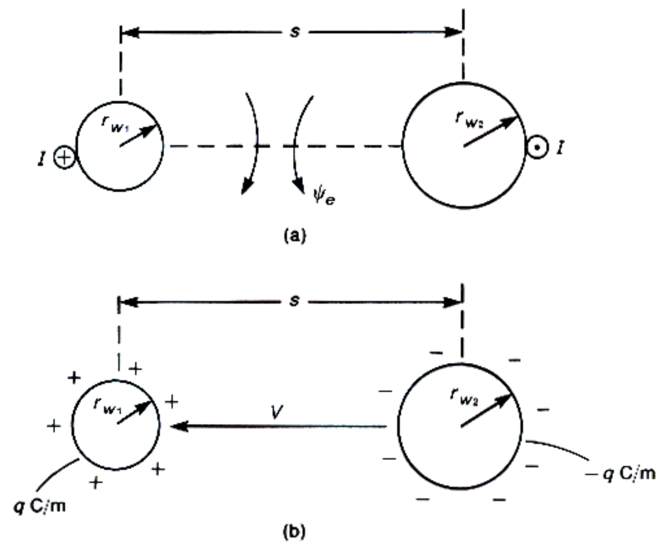


FIGURE 4.8 Determination of the per-unit-length parameters of a two-wire line: (a) inductance; (b) capacitance.

C = ? (by Q=C V)

L = ? (by Ψ=L I)

Analysis approach for Z_0 and T_d (Wires in air):

Ampere's Law for H field

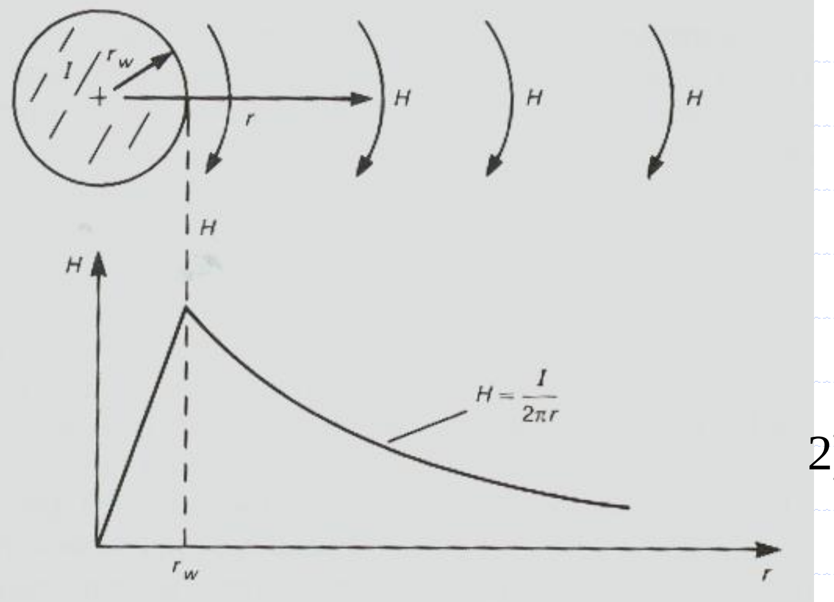


FIGURE 4.4 The magnetic field about a current-carrying wire.

$$H(r) = \frac{I}{\oint_c d\ell} = \frac{I}{2\pi r}$$

$$2)\quad \psi_e = \int_S \overrightarrow{B_T} \bullet d\vec{s} = \int_{r=R_1}^{R_2} \frac{\mu_0 I}{2\pi r} dr = \frac{\mu_0 I}{2\pi} \ln\left(\frac{R_1}{R_2}\right) \quad \text{(in Wb)}$$

Analysis approach for Z_0 and T_d (Wires in air):

Ampere's Law for H field

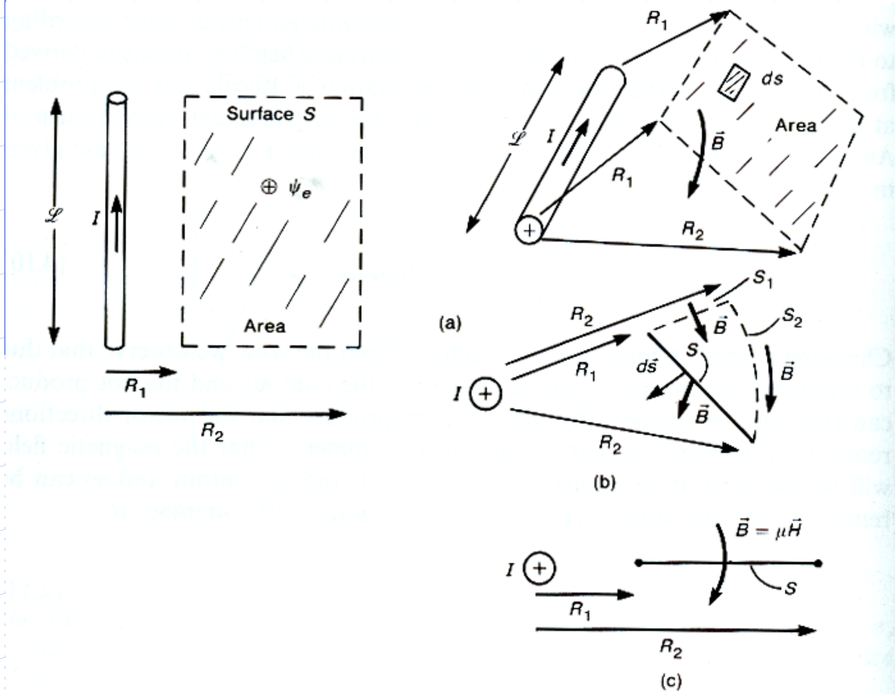


FIGURE 4.5 Illustration of a basic subproblem of determining the flux of a current through a surface: (a) dimensions of the problem; (b) use of Gauss' law; (c) an equivalent but simpler problem.

$$\psi_e = \frac{\mu_0 I}{2\pi} \ln\left(\frac{R_2}{R_1}\right)$$

$$L = \psi_e / I$$

The per-unit-length Parameters (E):

Gauss's Law

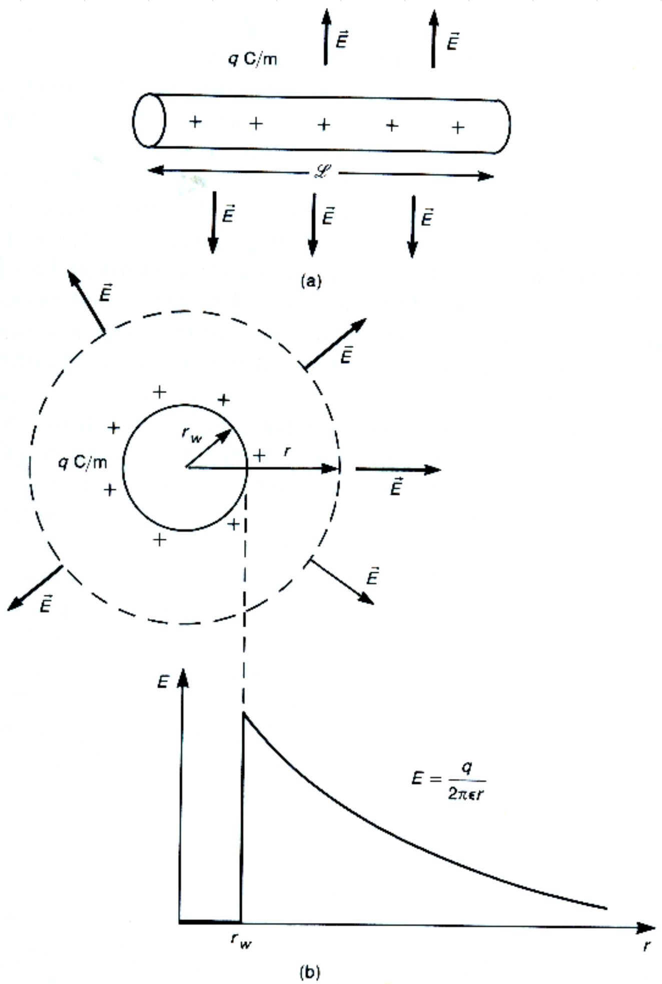


FIGURE 4.6 The electric field about a charge-carrying wire.

1) from gauss law

$$\nabla \bullet \vec{D} = \rho \Leftrightarrow \oint_S \varepsilon \vec{E_T} \bullet d\vec{s} = Q_{total}$$

$$\therefore E_T = \frac{q \times 1\text{m}}{\varepsilon_0 \oint_S ds}$$

$$= \frac{q}{2\pi\varepsilon_0 r}$$

2) $$\text{V} = \int_C \vec{\text{E}_\text{T}} \bullet d\vec{\ell} = -\int_{r=R_2}^{R_1} \frac{q}{2\pi\varepsilon_0 r} dr$$

$$= \frac{q}{2\pi\varepsilon_0} \ln \frac{\text{R}_2}{\text{R}_1}$$

The per-unit-length Parameters (E)

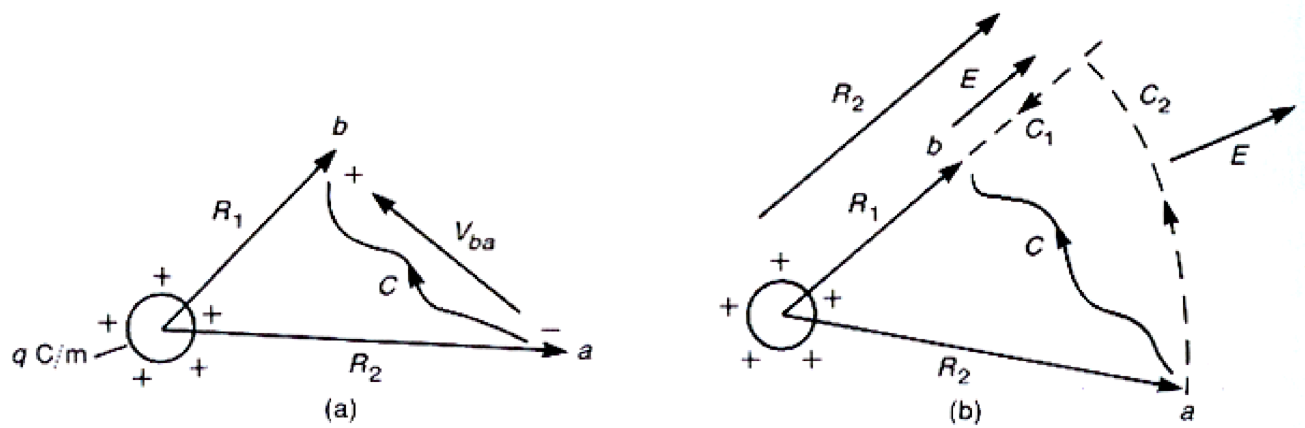


FIGURE 4.7 Illustration of a basic subproblem of determining the voltage between two points: (a) dimensions of the problem; (b) an equivalent but simpler problem.

$$V = \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{R_2}{R_1}\right)$$

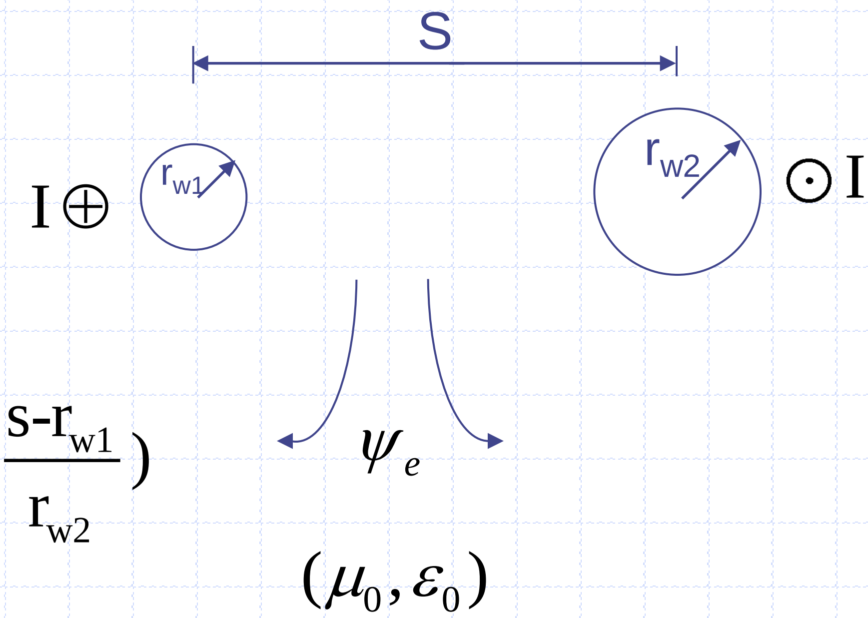
$$C = Q/V$$

c. For example Determine the L.C.G.R of the two-wire line.

(note：homogeneous medium)

Inductance：

$$L=\ell_e=\frac{\psi_e}{I}$$



where

$$\psi_e=\frac{\mu_0 I}{2\pi}\ln\left(\frac{s-r_{w2}}{r_{w1}}\right)+\frac{\mu_0 I}{2\pi}\ln\left(\frac{s-r_{w1}}{r_{w2}}\right)$$

$$=\frac{\mu_0 I}{2\pi}\ln\left(\frac{(s-r_{w2})(s-r_{w1})}{r_{w1}r_{w2}}\right)$$

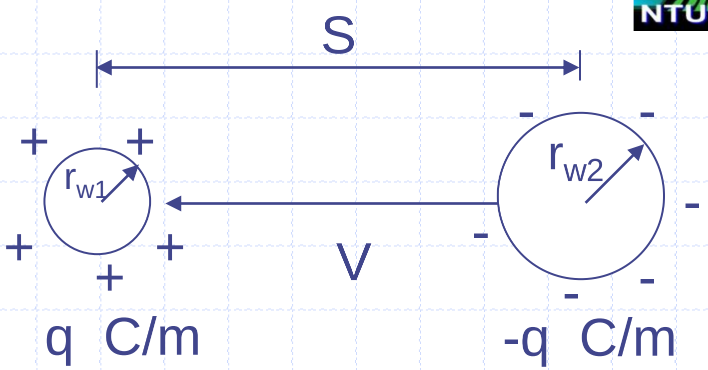
assume $s \gg r_{w1}$, r_{w2}

$$\Rightarrow L=\frac{\mu_0}{2\pi}\ln\left(\frac{s^2}{r_{w1}r_{w2}}\right)$$

Capacitance：

1) $\ell_e \bullet c = \mu_0 \varepsilon_0$

$$\Rightarrow C = \frac{2\pi\varepsilon_0}{\ln\left(\frac{s^2}{r_{w1} r_{w2}}\right)}$$



2) $$V = \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{s-r_{w2}}{r_{w1}}\right) + \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{s-r_{w1}}{r_{w2}}\right)$$

$$= \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{(s-r_{w2})(s-r_{w1})}{r_{w1} r_{w2}}\right)$$

$$\cong \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{s^2}{r_{w1} r_{w2}}\right) \quad \text{if } s \gg r_{w1}, r_{w2}$$

$$C = \frac{q}{V} = \frac{2\pi\varepsilon_0}{\ln\left(\frac{s^2}{r_{w1} r_{w2}}\right)}$$ ← the same with 1) approach

The per-unit-length Parameters

Homogeneous structure

TEM wave structure is like the DC (static) field structure

$$LG = \mu\sigma$$

$$LC = \mu\varepsilon$$

So, if you can derive how to get the L, G and C can be obtained by the above two relations.

The per-unit-length Parameters (Above GND)

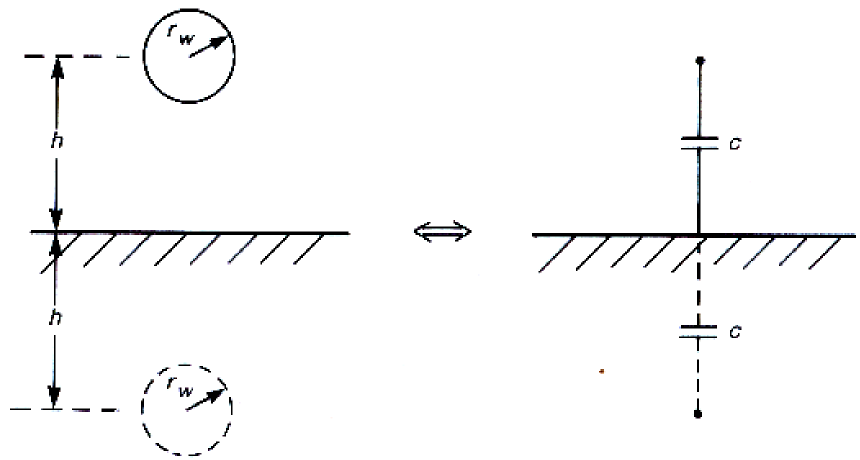


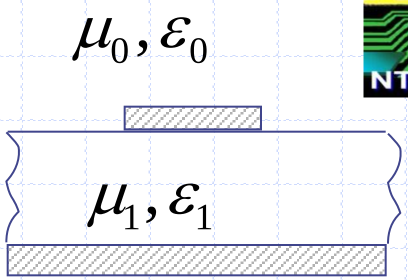
FIGURE 4.9 Determination of the per-unit-length capacitance of a wire above a ground plane with the method of images.

2C

L/2

Why?

d. How to determine L,C for microstrip-line.



1) This is inhomogeneous medium.
2) Nunerical method should be used to solve the C of this structure, such as Finite element, Finite Difference...
3) But ℓ_e can be obtained by

$$\ell_e C_0 = \mu_0 \varepsilon_0 \quad \Rightarrow \quad \ell_e = \frac{\mu_0 \varepsilon_0}{C_0}$$

where C_0 is the capacitance when ε_1 medium is replaced by ε_0 medium.

Analysis approach for Z_0 and T_d (Strip line)

Approximate electrostatic solution

1. 

2. The fields in TEM mode must satisfy Laplace equation

$$\nabla_t^{\,2}\Phi(x,y) = 0$$

where Φ is the electric potential

The boundary conditions are

$$\Phi(x,y) = 0 \quad \text{at } x = \pm a/2$$

$$\Phi(x,y) = 0 \quad \text{at } \; y = 0, b$$

Analysis approach for Z_0 and T_d

3. Since the center conductor will contain the surface charge, so

$$\Phi(x,y)=\begin{cases}\displaystyle\sum_{\substack{n=1\\ odd}}^{\infty} A_n \cos\frac{n\pi x}{a}\sinh\frac{n\pi y}{a} & \text{for } 0\le y\le b/2\\ \displaystyle\sum_{\substack{n=1\\ odd}}^{\infty} B_n \cos\frac{n\pi x}{a}\sinh\frac{n\pi}{a}(b-y) & \text{for } b/2\le y\le b\end{cases}$$

Why?

4. The unknowns A_n and B_n can be solved by two known conditions:

$$\begin{cases}\text{The potential at } y=b/2 \text{ must continuous}\\ \text{The surface charge distribution for the strip: } \rho_s=\begin{cases}1 & \text{for } |x|\le W/2\\ 0 & \text{for } |x|\ge W/2\end{cases}\end{cases}$$

Analysis approach for Z_0 and T_d

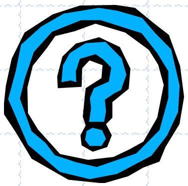
5.
$$\begin{cases} V = -\int_0^{b/2} E_y(x=0,y)dy = -\int_0^{b/2} -\partial\Phi(x,y)/\partial y(x=0,y)dy \\ Q = \int_{-w/2}^{w/2} \rho_s(x)dx = W(C/m) \end{cases}$$

6.
$$C = \frac{Q}{V} = \frac{W}{\displaystyle\sum_{\substack{n=1 \\ odd}}^{\infty} \frac{2a\sin(n\pi W/2a)\sinh(n\pi b/2a)}{(n\pi)^2 \varepsilon_0 \varepsilon_r \cosh(n\pi b/2a)}}$$

$$Z_0 = \frac{1}{v_p C} = \frac{\sqrt{\varepsilon_r}}{cC}$$

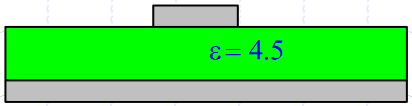
Answers!!

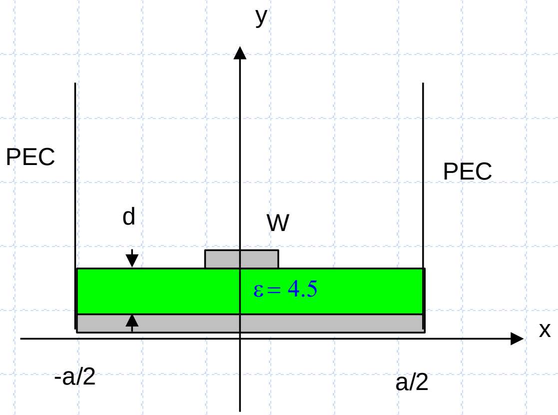
7.
$$T_d = \sqrt{\varepsilon_r}/c$$



Analysis approach for Z_0 and T_d (Microstrip Line)

1.





2. The fields in Quasi - TEM mode must satisfy Laplace equation

$$\nabla_t^{\ 2}\Phi(x, y) = 0$$

where Φ is the electric potential

The boundary conditions are

$$\Phi(x, y) = 0 \ \text{ at } x = \pm a/2$$

$$\Phi(x, y) = 0 \ \text{ at } \ y = 0, \infty$$

Analysis approach for Z_0 and T_d (Microstrip Line)

3. Since the center conductor will contain the surface charge, so

$$\Phi(x,y)=\begin{cases}\displaystyle\sum_{\substack{n=1\\odd}}^{\infty} A_n \cos\frac{n\pi x}{a}\sinh\frac{n\pi y}{a} & \text{for } 0\le y\le d\\ \displaystyle\sum_{\substack{n=1\\odd}}^{\infty} B_n \cos\frac{n\pi x}{a}e^{-n\pi y/a} & \text{for } d\le y\le\infty\end{cases}$$

4. The unknowns A_n and B_n can be solved by two known conditions and the orthogonality of *cos* function :

$$\begin{cases}\text{The potential at } y=d \text{ must continuous}\\ \text{The surface charge distribution for the strip: } \rho_s=\begin{cases}1 & \text{for } |x|\le W/2\\ 0 & \text{for } |x|\ge W/2\end{cases}\end{cases}$$

Analysis approach for Z_0 and T_d (Microstrip Line)

5.
$$\begin{cases} V = -\int_0^{b/2} E_y(x=0,y)dy = -\int_0^{b/2} -\partial\Phi(x,y)/\partial y(x=0,y)dy = \sum_{\substack{n=1 \\ odd}}^{\infty} A_n \sinh\frac{n\pi d}{a} \\ Q = \int_{-w/2}^{w/2} \rho_s(x)dx = W(C/m) \end{cases}$$

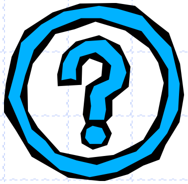
6.
$$C = \frac{Q}{V} = \frac{W}{\sum_{\substack{n=1 \\ odd}}^{\infty} \frac{4a\sin(n\pi W/2a)\sinh(n\pi d/2a)}{(n\pi)^2 W\varepsilon_0[\sinh(n\pi d/a)+\varepsilon_r\cosh(n\pi d/a)]}}$$

Analysis approach for Z_0 and T_d (Microstrip Line)

7. To find the effective dielectric constant ε_e, we consider two cases of capacitance

1. C = capacitance per unit length of the microstrip line with the dielectric substrate $\varepsilon_r \neq 1$
2. C_0 = capacitance per unit length of the microstrip line with the dielectric substrate $\varepsilon_r = 1$

$$\therefore \varepsilon_e = \frac{C}{C_0}$$



8.

$$Z_0 = \frac{1}{v_p C} = \frac{\sqrt{\varepsilon_e}}{cC}$$

$$T_d = \sqrt{\varepsilon_e} / c$$

Tables for Z_0 and T_d (Microstrip Line)

Z_0 (Ω)	20	28	40	50	75	90	100
ε_{eff}	3.8	3.68	3.51	3.39	3.21	3.13	3.09
L_0 (nH / mm)	0.119	0.183	0.246	0.320	0.468	0.538	0.591
C_0 (pF / mm)	0.299	0.233	0.154	0.128	0.083	0.067	0.059
T_0 (ps / mm)	6.54	6.41	6.25	6.17	5.99	5.92	5.88

Fr4 : dielectric constant = 4.5
Frequency: 1GHz

Tables for Z_0 and T_d (Strip Line)

Z_0 (Ω)	20	28	40	50	75	90	100
ε_{eff}	4.5	4.5	4.5	4.5	4.5	4.5	4.5
L_0 (nH / mm)	0.141	0.198	0.282	0.353	0.53	0.636	0.707
C_0 (pF / mm)	0.354	0.252	0.171	0.141	0.094	0.078	0.071
T_0 (ps / mm)	7.09	7.09	7.09	7.09	7.09	7.09	7.09

Fr4 : dielectric constant = 4.5
Frequency: 1GHz

Analysis approach for Z_0 and T_d (EDA/Simulation Tool)

1. HP Touch Stone (HP ADS)
2. Microwave Office
3. Software shop on Web:
4. APPCAD

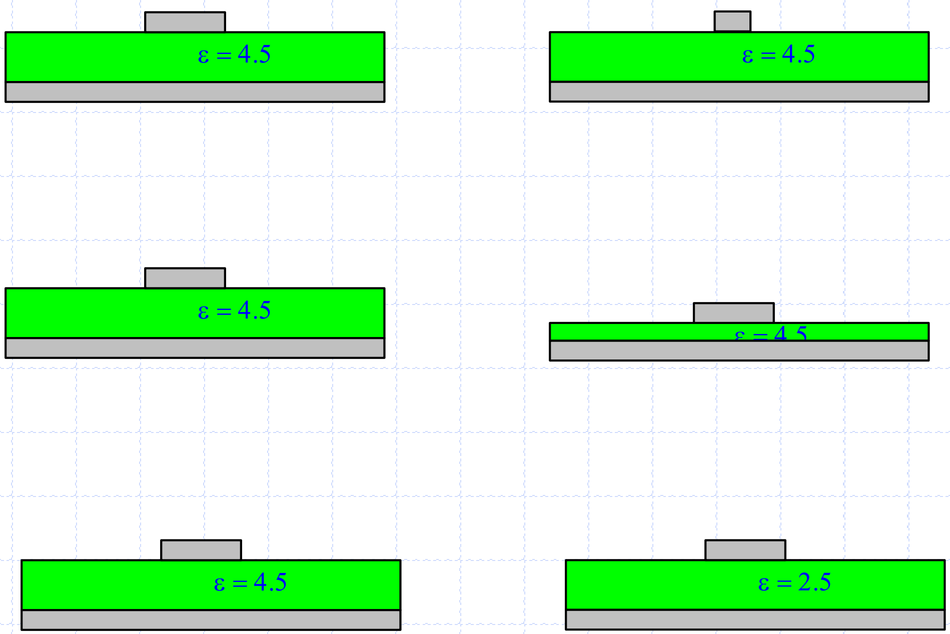
(http://softwareshop.edtn.com/netsim/si/termination/term_article.html)

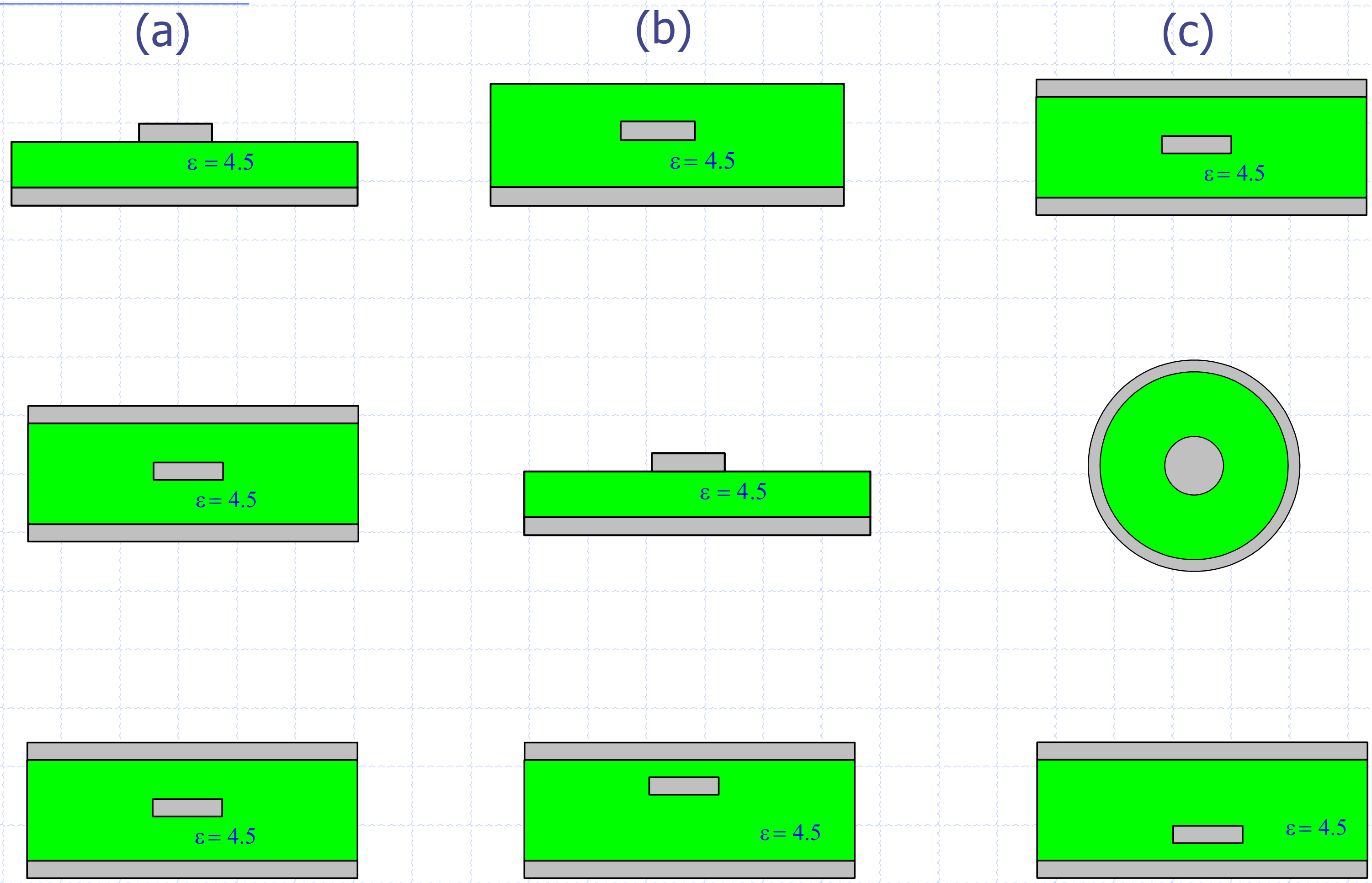
(http://www.agilent.com/view/rf or http://www.hp.woodshot.com)

Concept Test for Planar Transmission Lines

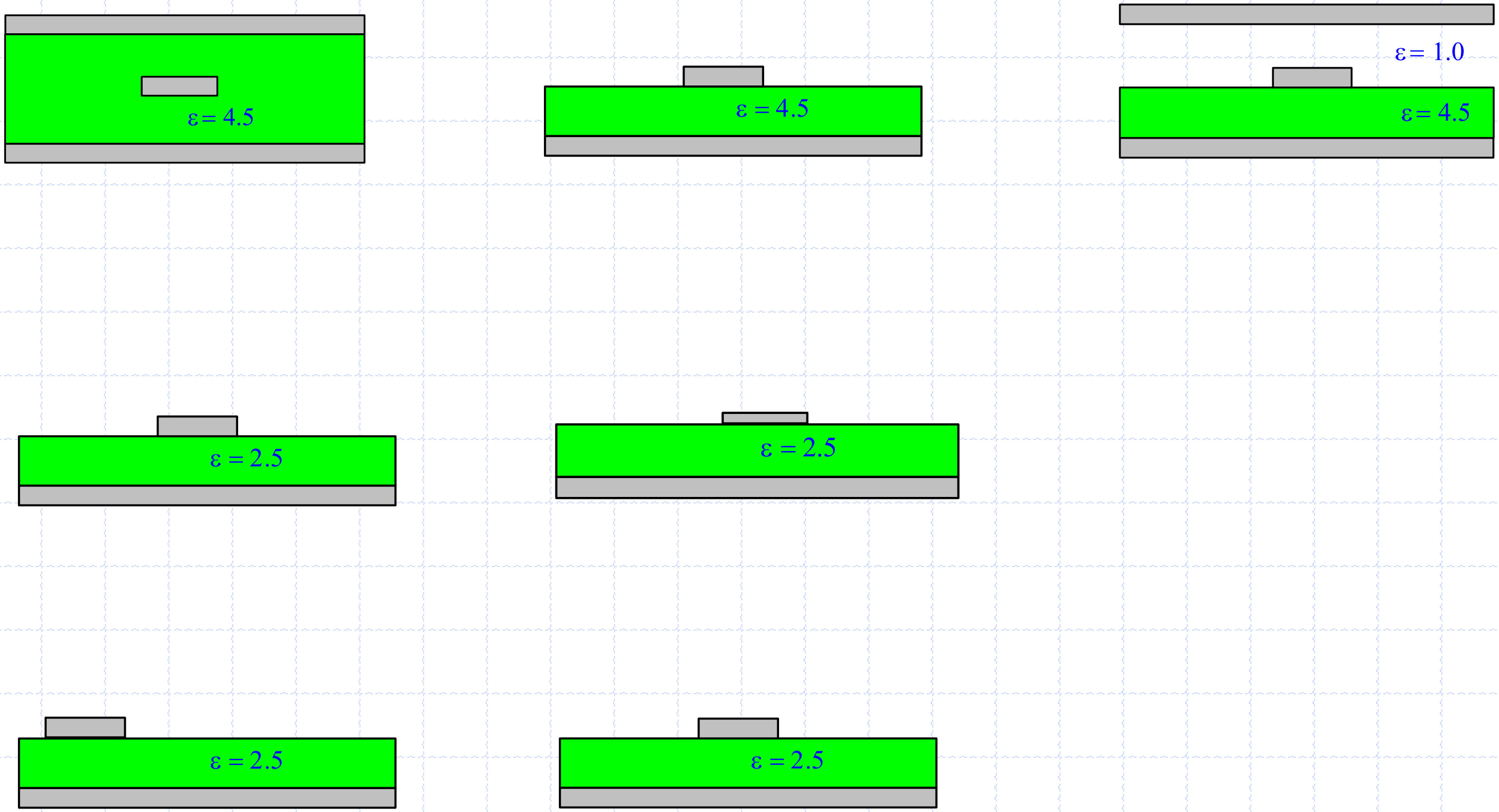
- Please compare their Z_0 and V_p

(a) (b)




(a)
(b)
(c)
ε = 4.5
ε = 4.5
ε = 4.5
ε = 4.5
ε = 4.5
ε = 4.5
ε = 4.5
ε = 4.5

(a) (b) (c)



Loss of Transmission Lines

Typically, dielectric loss is quite small -> $G_0 = 0$. Thus

$$Z_0 = \sqrt{\frac{R_0 + jwL_0}{jwC_0}} = \sqrt{\frac{L_0}{C_0}}(1 - jx)^{1/2}$$

$$r = \sqrt{(R_0 + jwL_0)(jwC_0)} = \alpha + j\beta$$

where $x = \dfrac{R_0}{wL_0}$

$w = \dfrac{R_0}{L_0}$

Highly Lossy ← ↓ → **Near Lossless**

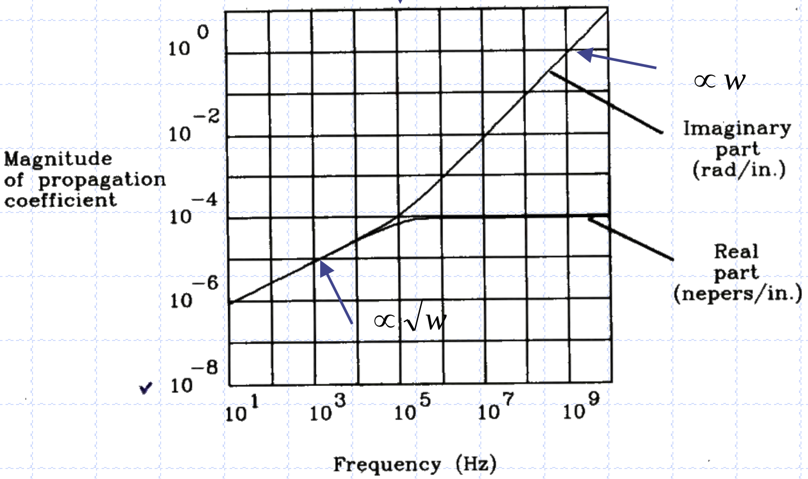


Figure 4.9 Propagation of a cable with fixed series resistance (no skin effect).

- Lossless case : $x = 0$
- Near Lossless: $x << 1$
- Highly Lossy: $x >> 1$

Loss of Transmission Lines

- For Lossless case:

$$\alpha = 0$$

$$\beta = \omega\sqrt{L_0 C_0}$$

$$Z_0 = \sqrt{\frac{L_0}{C_0}}$$

$$\text{Time delay } T_0 = \sqrt{L_0 C_0}$$

- For Near Lossless case:

$$\alpha \approx \frac{R_0}{2\sqrt{L_0 / C_0}}$$

$$\beta \approx \omega\sqrt{L_0 C_0}\left[1 - \frac{x^2}{8}\right]$$

$$Z_0 \cong \sqrt{\frac{L_0}{C_0}}\left(1 - j\frac{R_0}{2wL_0}\right) = \sqrt{\frac{L_0}{C_0}} + \frac{1}{jwC} \text{ where } C = 2T_0 / R_0$$

$$\text{Time delay } T_0 = \sqrt{L_0 C_0}$$

Loss of Transmission Lines

- For highly loss case: (RC transmission line)

$$\alpha \approx \sqrt{\frac{wR_0C_0}{2}}[1-\frac{1}{2x}]$$

$$\beta \approx \sqrt{\frac{wR_0C_0}{2}}[1+\frac{1}{2x}]$$

$$Z_0 \approx \sqrt{\frac{R_0}{2wC_0}}[1+\frac{1}{2x}]$$

Nonlinear phase relationship with f introduces signal distortion

Example of RC transmission line:
AWG 24 telephone line in home

$$Z_0(w) = \left(\frac{R+iwL}{jwC}\right)^{1/2} = 648(1+j)$$

where

$R = 0.0042\Omega / in$

$L = 10nH / in$

$C = 1pF / in$

$w = 10{,}000 rad / s (1600 Hz)$: voice band

That's why telephone company terminate the lines with 600 ohm

Loss of Transmission Lines (Dielectric Loss)

TABLE 5.3 SOME TYPICAL LINE PARAMETERS

Case	L_o (nH/cm)	C_o (pF/cm)	R_o (Ω/cm)	Z_o (Ω)	T_o (ps/cm)	ϵ_r	$R_o/\omega L_o$ [a]
PCB	5	1	0.050[b]	70.7	70.7	4.5	0.0023
MCM	5	1	5	70.7	70.7	4.5	0.23
Chip	2.2	2	500	32.9	65.8	3.9	52.5

[a] $\omega = 2\pi f = 2\pi(0.35)/T_r = 4.4 \times 10^9$ radian at $T_r = 0.5$ ns.
[b] 4-mil width, 1-oz Cu.

The loss of dielectric loss is described by the loss tangent

$$\tan\delta_D = \frac{G}{wC}$$

FR4 PCB $\tan\delta_D = 0.035$

$$\therefore \alpha_D = \frac{GZ_0}{2} = (wC\tan\delta_D Z_0)/2 = \pi f \tan\delta_D \sqrt{LC}$$

Loss of Transmission Lines (Skin Effect)

- Skin Effect

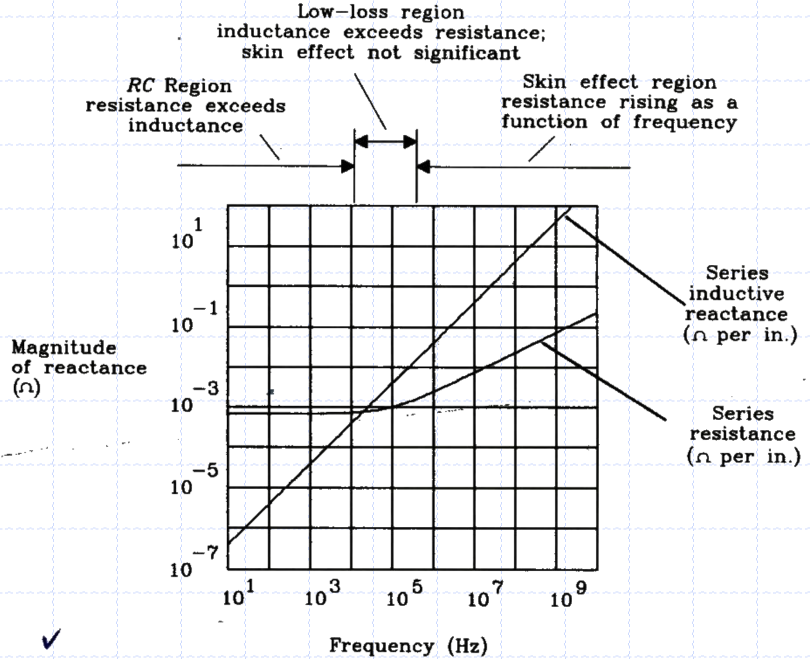


Figure 4.10 Series resistance and series inductive reactance of RG-58/U coax versus frequency.

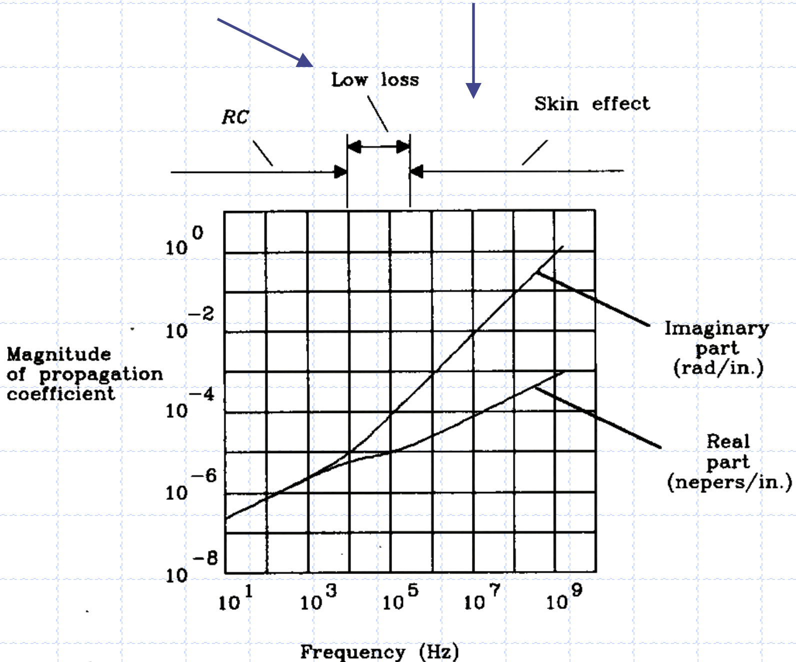


Figure 4.11 Propagation coefficient of RG-58/U includes skin effect.

Loss of Transmission Lines (Skin Effect)

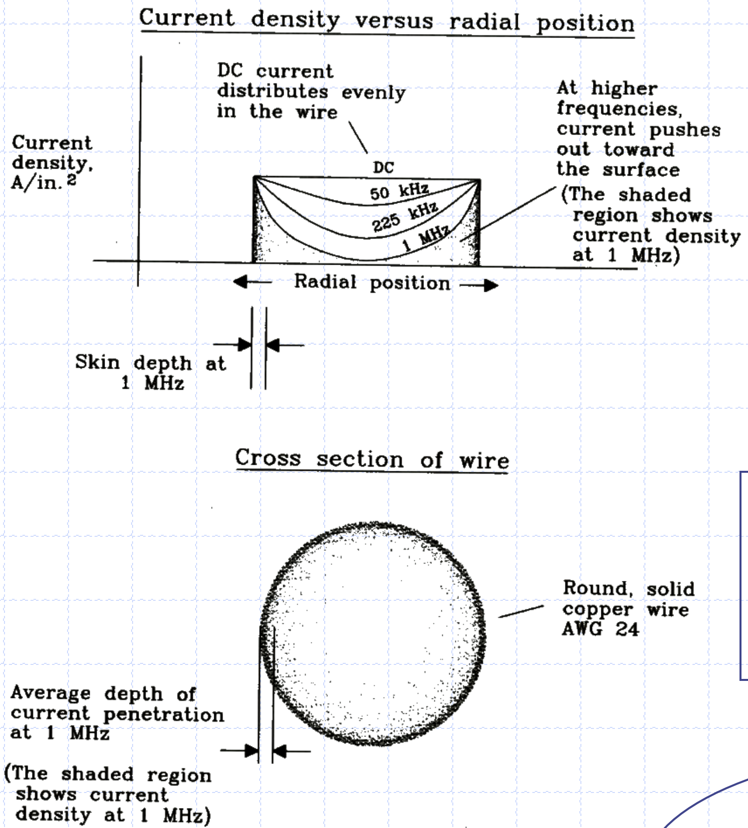


Figure 4.12 Distribution of current in a round wire.

$$\delta_s = \frac{1}{\alpha} = \sqrt{\frac{2}{w\mu\sigma}}$$

$$R(w) = \frac{1}{\sigma}\left(\frac{\text{length}}{\text{area}}\right) \propto \sqrt{\frac{w}{\sigma}}$$

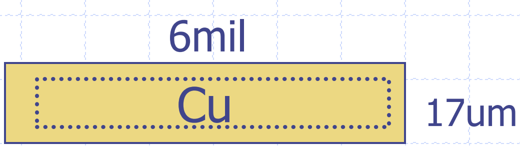
NOTE: In the near lossless region ($R / wL << 1$), the characteristic impedance Z_0 is not much affected by the skin effect

$\because\ R(w) \propto \sqrt{w}$

$\therefore\ R(w) / wL \propto (1/\sqrt{w}) << 1$

Loss of Transmission Lines (Skin Effect)

f (MHz)	100	200	400	800	1200	1600	2000
$\delta_s = \sqrt{\frac{1}{f\mu\sigma}}$	6.6um	4.7um	3.3um	2.4um	1.9um	1.7um	1.5um
$R_s\,(\Omega)$	2.6m ohm	3.7m ohm	5.2m ohm	7.4m ohm	9.0m ohm	10.8m ohm	11.6m ohm
Trace resistance	1.56 ohm	2.22 ohm	3.12 ohm	4.44 ohm	5.4 ohm	6.48 ohm	7.0 ohm



Skin depth resistance $R_s = \sqrt{\frac{\pi\mu f}{\sigma}}\,(\Omega)$

$\mu = 4\pi \times 10^{-7}\ H/m$

$\sigma(\mathrm{Cu}) = 5.8 \times 10^{7}\ S/m$

Length of trace = 20cm

Loss Example: Gigabit differential transmission lines

For comparison: (Set Conditions)

1. Differential impedance = 100
2. Trace width fixed to 8mil
3. Coupling coefficient = 5%
4. Metal : 1 oz Copper

Question:

1. Which one has larger loss by skin effect?
2. Which one has larger loss of dielectric?

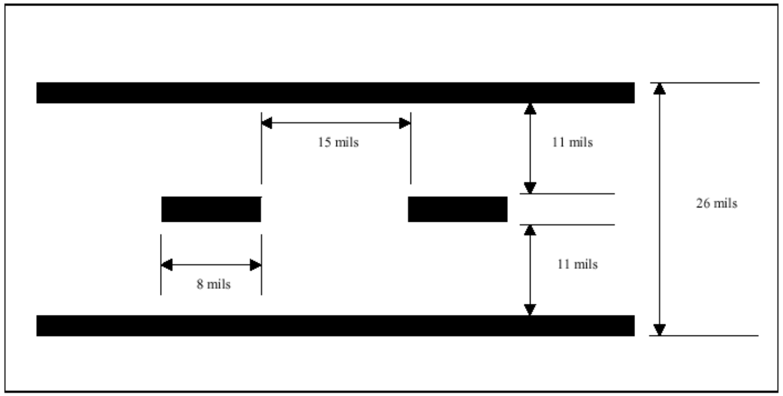


Figure 14 - Single Stripline Coplanar Geometry

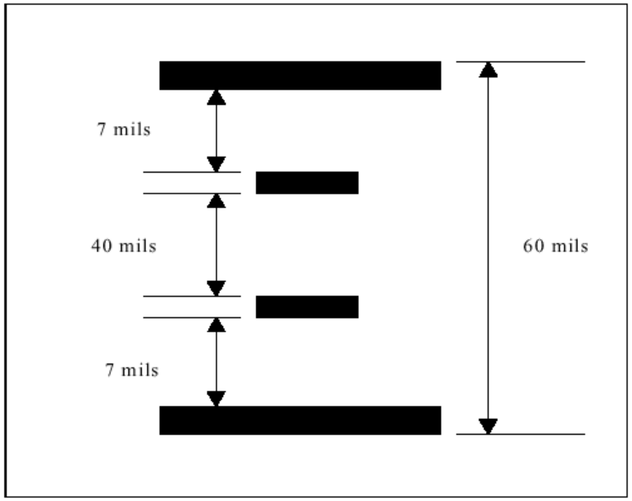


Figure 15 - Dual Stripline Geometry

Loss Example: Gigabit differential transmission lines

Skin effect loss

Frequency	Stripline Resistance Ω / feet	Dual Stripline Resistance Ω / feet	Percent Difference
500 MHz	6.144	6.648	8.2%
1.5 GHz	10.668	11.508	7.9%
2.5 GHz	13.728	14.832	8.0%

Table 3 - Simulated Results of Skin Effect Losses

Loss Example: Gigabit differential transmission lines

Skin effect loss

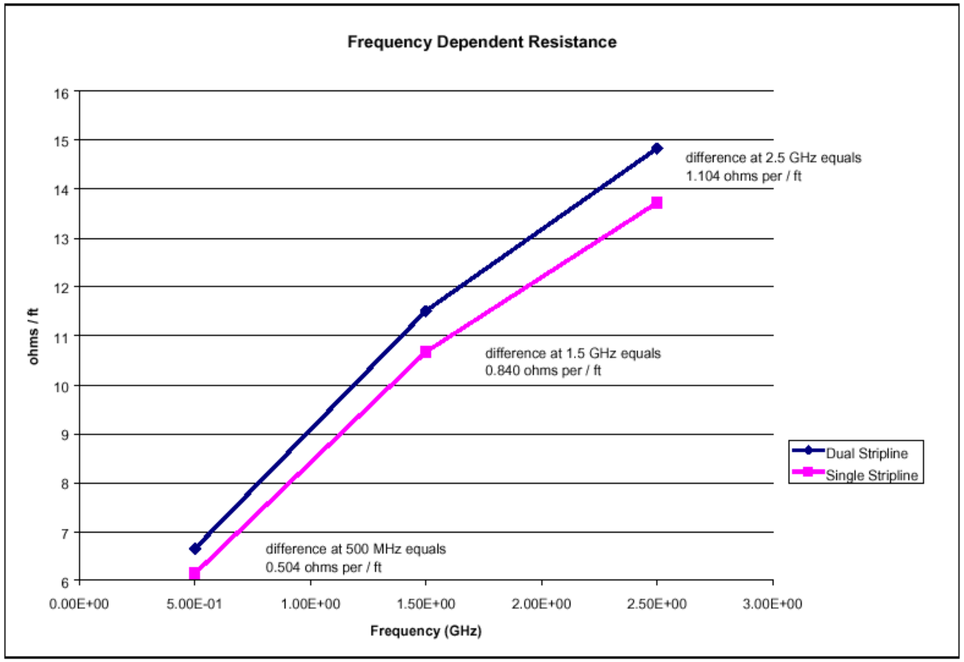


Figure 18 - Graph of Simulated Results of Skin Effect Losses

Why?

Loss Example: Gigabit differential transmission lines

Look at the field distribution of the common-mode coupling

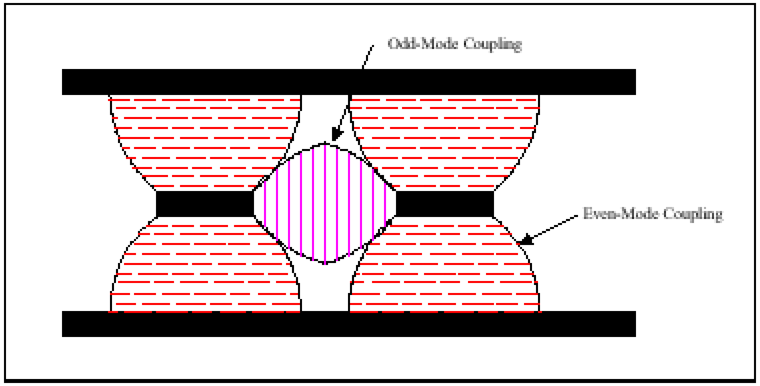


Figure 11 - Coplanar Differential Single Stripline Routing Geometry

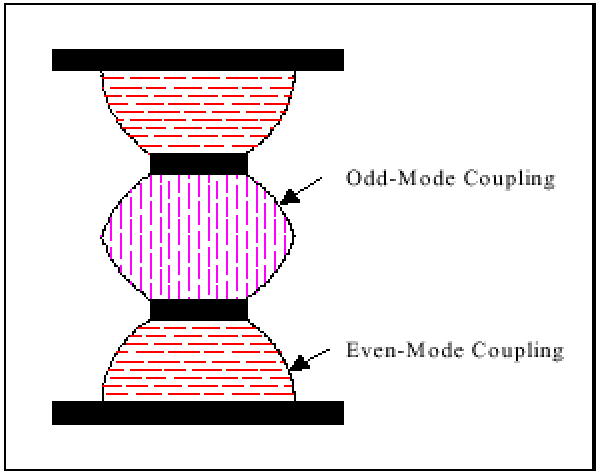


Figure 12 - Differential Routing in a Dual Stripline Geometry

Coplanar structure has more surface for current flowing

Loss Example: Gigabit differential transmission lines

How about the dielectric loss ? Which one is larger?

Loss Example: Gigabit differential transmission lines

The answer is dual stripline has larger loss. Why ?

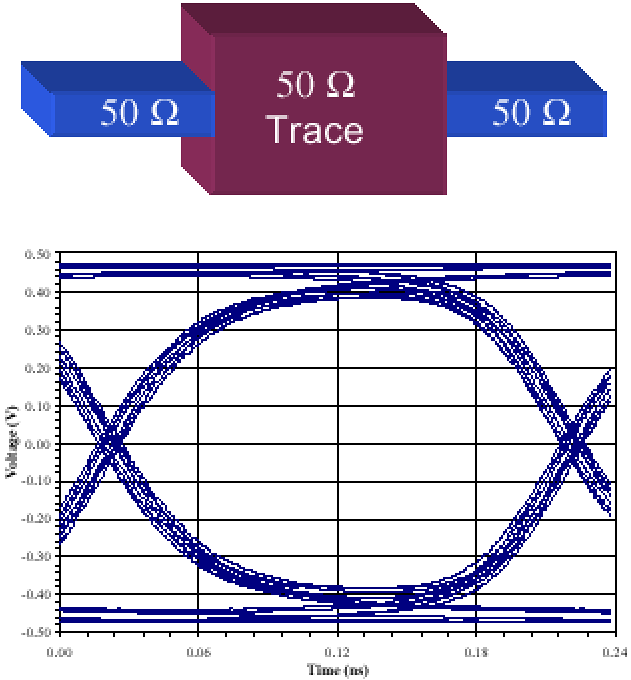
The field density in the dielectric between the trace and GND is higher for dual stripline.

Loss Example: Gigabit differential transmission lines

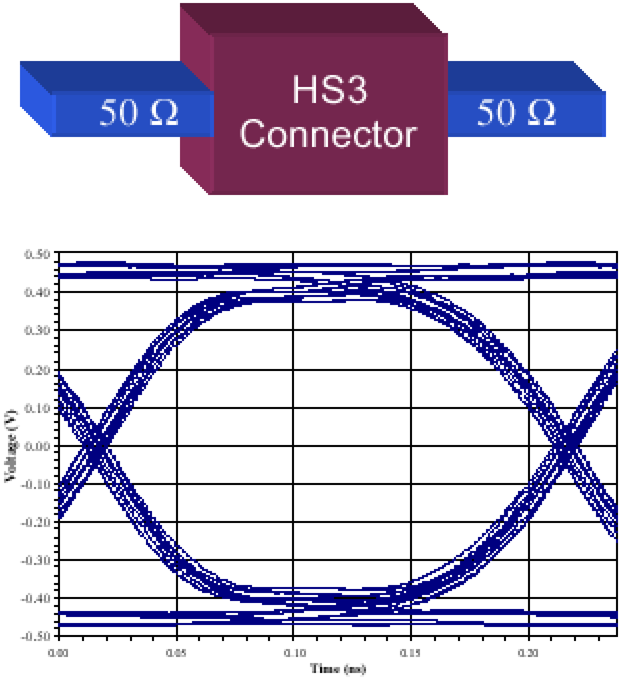
Which one has higher ability of rejecting common-mode noise ?

Loss Example: Gigabit differential transmission lines

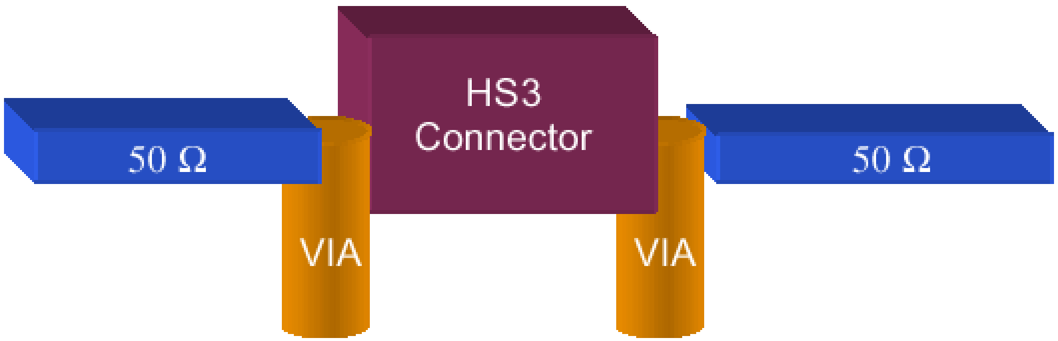
The answer is coplanar stripline. Why ?

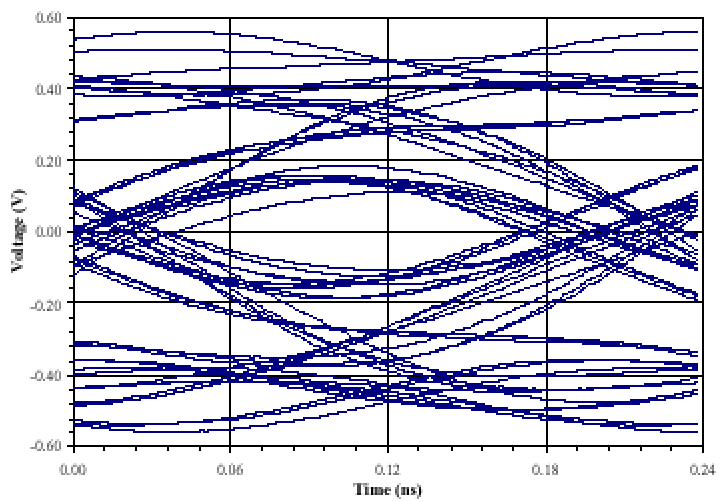


769 mV Opening, 6.25% Jitter



754 mV Opening, 6.25% Jitter





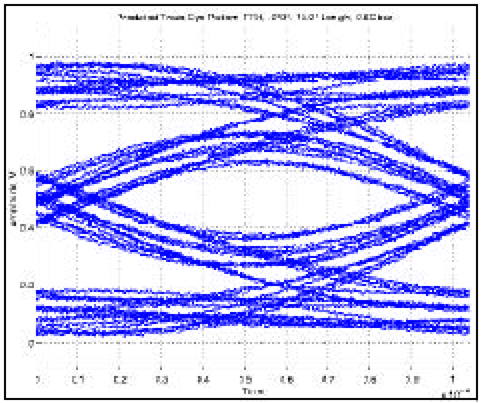
218 mV Opening, 34.4% Jitter

-The output waveform shown results from a 1-volt, 32-bit inverting K28.5 input bit pattern (5 Gbps, 60ps edges) that is applied to a system with two through-holes, two AMP HS3 connectors, and a 12 mil, 50 Ohm stripline trace that is ~18" long.

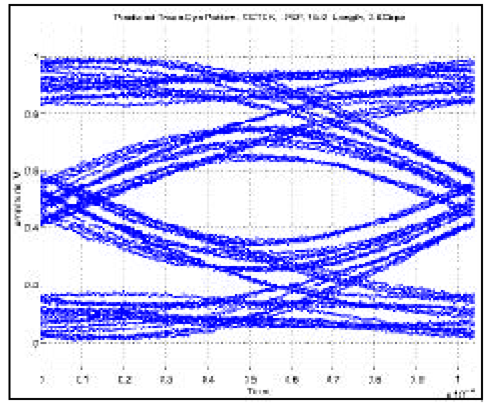
Material	ε_r* @ 1 MHz	ε_r* @ 1 GHz	$\tan\delta$* @ 1 GHz	Relative Cost**
FR4	4.30	4.05	0.020	1
GETEK	4.15	4.00	0.015	1.1
ROGERS 4350/4320	3.75	3.60	0.009	2.1
ARLON CLTE	3.15	3.05	0.004	6.8

* Measured from test data
**Cost factor derived from 10" by 20", 12-layer backplane

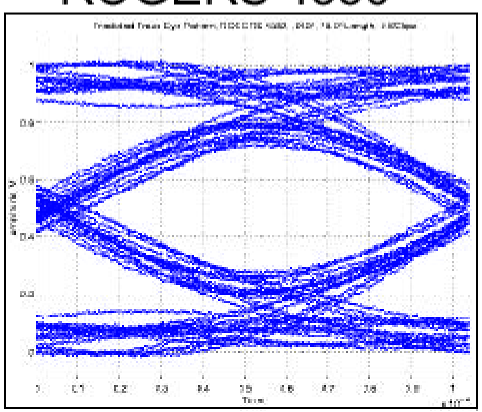
FR4



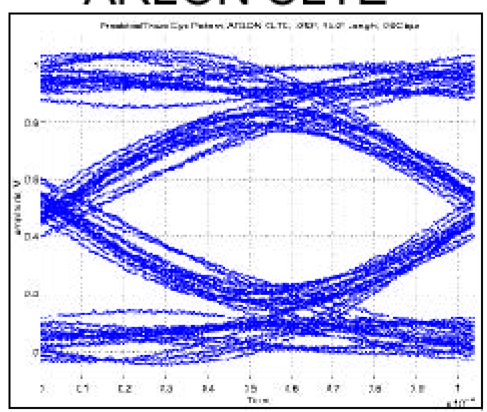
GETEK



ROGERS 4350



ARLON CLTE



FR4:
Jitter = 0.30 UI
Opening = 238 mV

GETEK:
Jitter = 0.28 UI
Opening = 268 mV

ROGERS 4350:
Jitter = 0.20 UI
Opening = 426 mV

ARLON CLTE:
Jitter = 0.19 UI
Opening = 520 mV

-The output waveforms shown result from a 1-volt, 32-bit inverting K28.5 input bit pattern (10 Gbps, 60ps edges) that is applied to a 12 mil, 50 Ohm stripline trace that is 18" long.

Intuitive concept to determine Z_0 and T_d

- How physical dimensions affect impedance and delay

Sensitivity is defined as percent change in impedance per percent change in line width, *log-log plot* shows sensitivity directly.

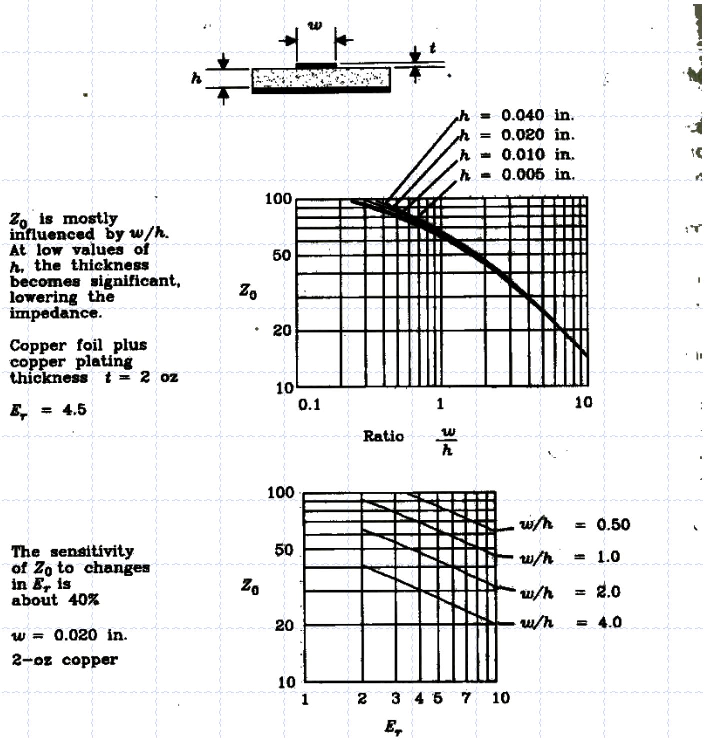


Figure 4.31 Characteristic impedance of a microstrip transmission line versus geometry and permittivity. (See formulas in Appendix C.)

Z_0 is mostly influenced by w / h, the sensitivity is about 100%.

It means 10% change in w / h will cause 10% change of Z_0

The sensitivity of Z_0 to changes in ε_r is about 40%

Intuitive concept to determine Z_0 and T_d

- Striplines

impedance

Delay

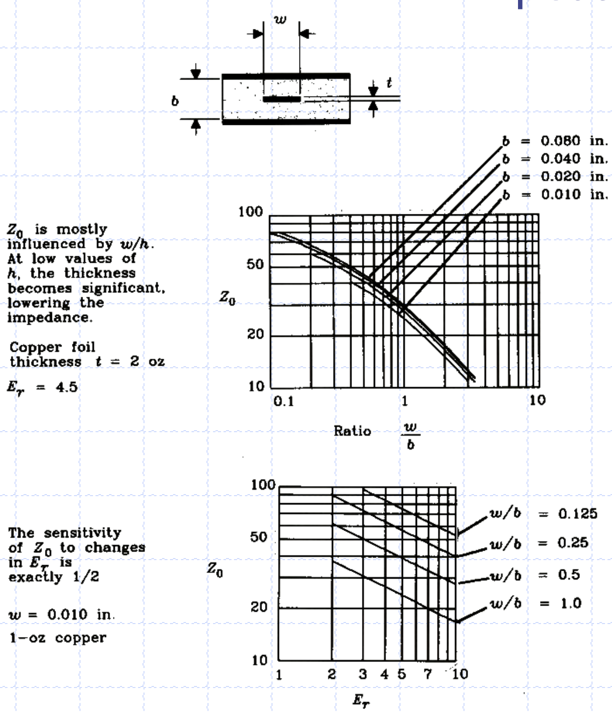


Figure 4.33 Characteristic impedance of a stripline transmission line versus geometry and permittivity. (See formulas in Appendix C.)

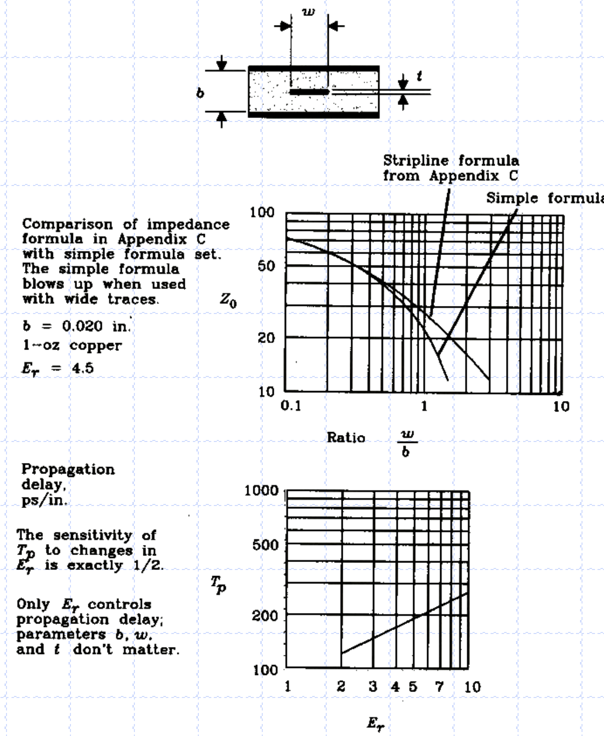


Figure 4.34 Characteristic impedance of a stripline transmission line.

Ground Perforation: BGA via and impedance

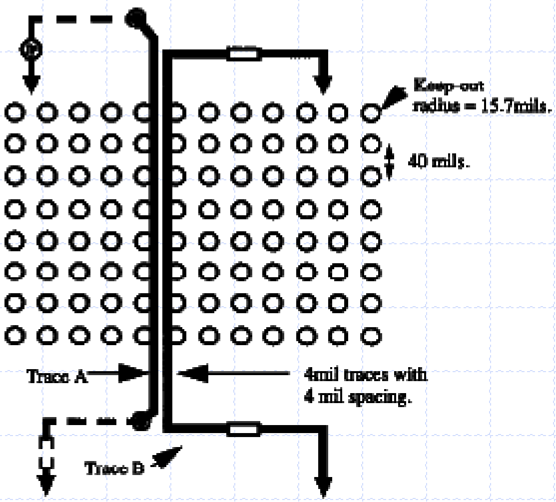


Figure 1. *Section of a typical 1600pin BGA pin field with signal traces running through. Drawing is not to scale.*

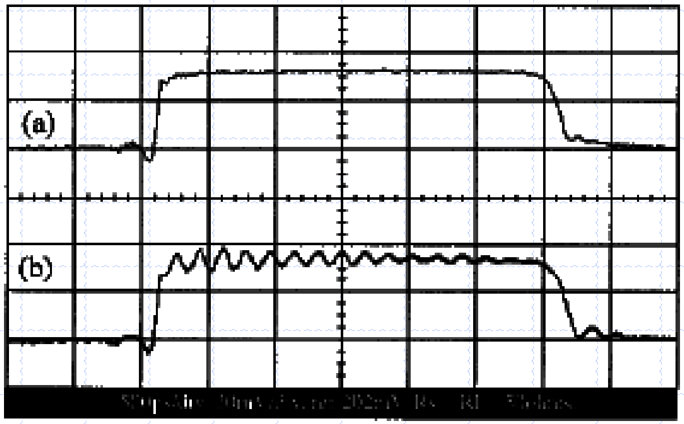


Figure 2: *Characteristic Impedance measurements for a 68.8ohm (ideal value) trace over (a) solid reference plane, and (b)perforated reference plane.*

Ground Perforation: Cross-talk (near end)

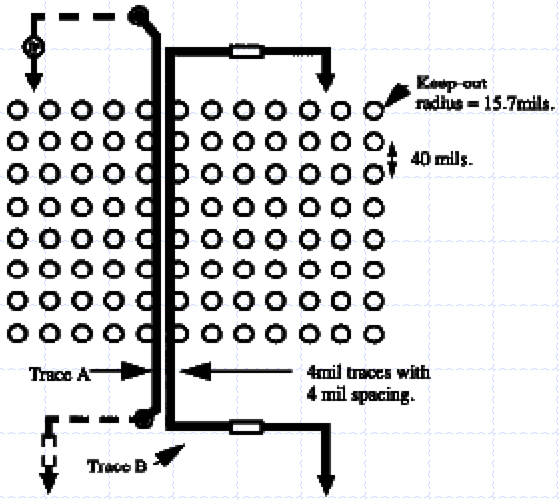


Figure 1. *Section of a typical 1600pin BGA pin field with signal traces running through. Drawing is not to scale.*

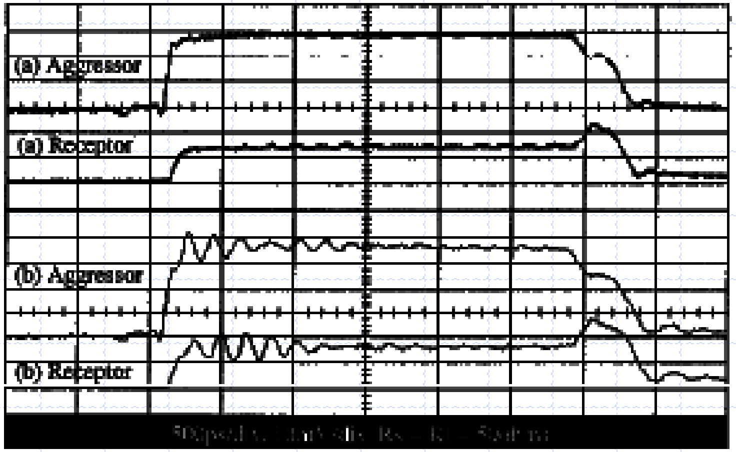


Figure 3: *Near-end crosstalk measured for (a) solid reference plane and (b) perforated reference plane with both ends of Trace B terminated in 50ohm.*

Ground Perforation : Cross-talk (far end)

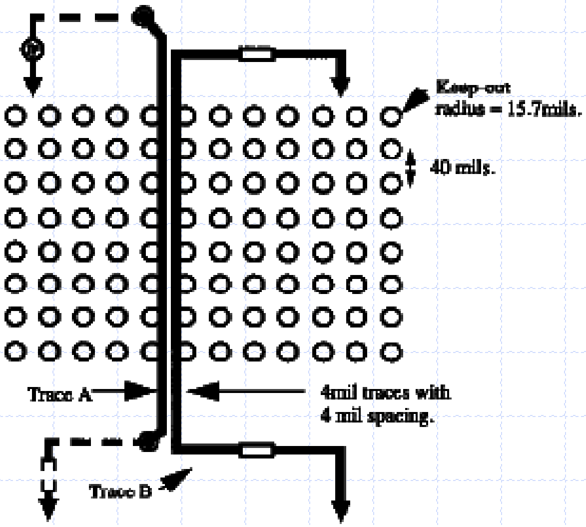


Figure 1. *Section of a typical 1600pin BGA pin field with signal traces running through. Drawing is not to scale.*

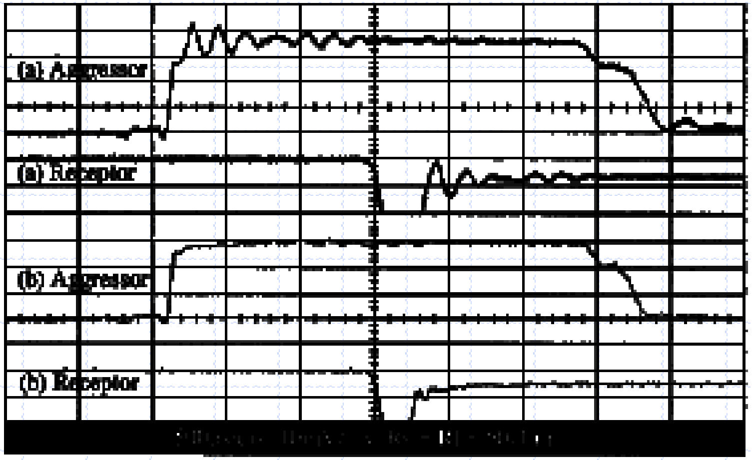
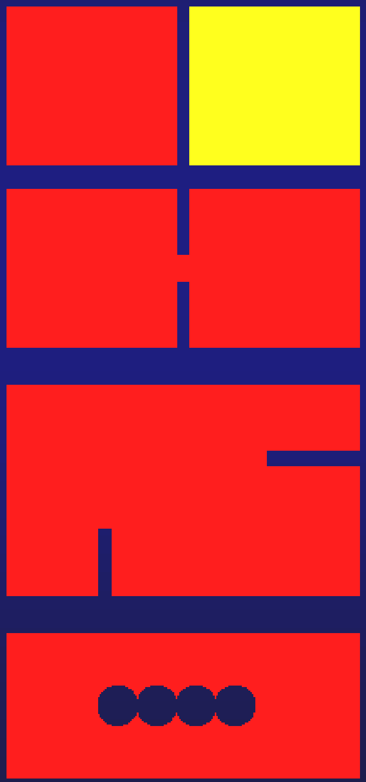


Figure 4: *Far-end crosstalk measured for (a) perforated reference plane and (b) solid reference plane with both ends of Trace B terminated in 50ohm.*

Example(II): Transmission line on non-ideal GND

Reasons for splits or slits on GND planes

- DC isolation between different supply voltages.
- AC isolation of digital from low noise analog circuits.
- Low cost method of removing unwanted resonances from the power distribution system.
- Nearby touching via holes.



Example(II): Transmission line on non-ideal GND

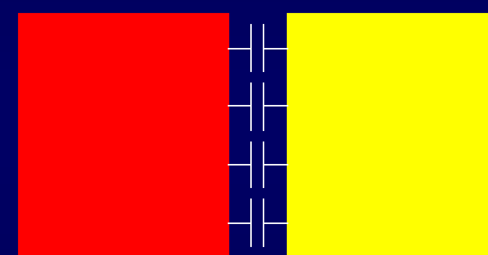
Disadvantages of Image Plane Slits and Splits

- Transverse slits in the image planes present a discontinuity to the flow of AC currents.
- Result in significant signal degradation.
- Help generate common mode currents that result in significant radiation.

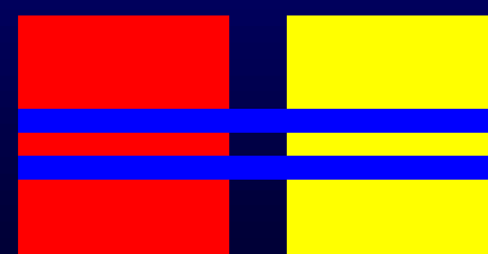
Example(II): Transmission line on non-ideal GND

Two most commonly used:

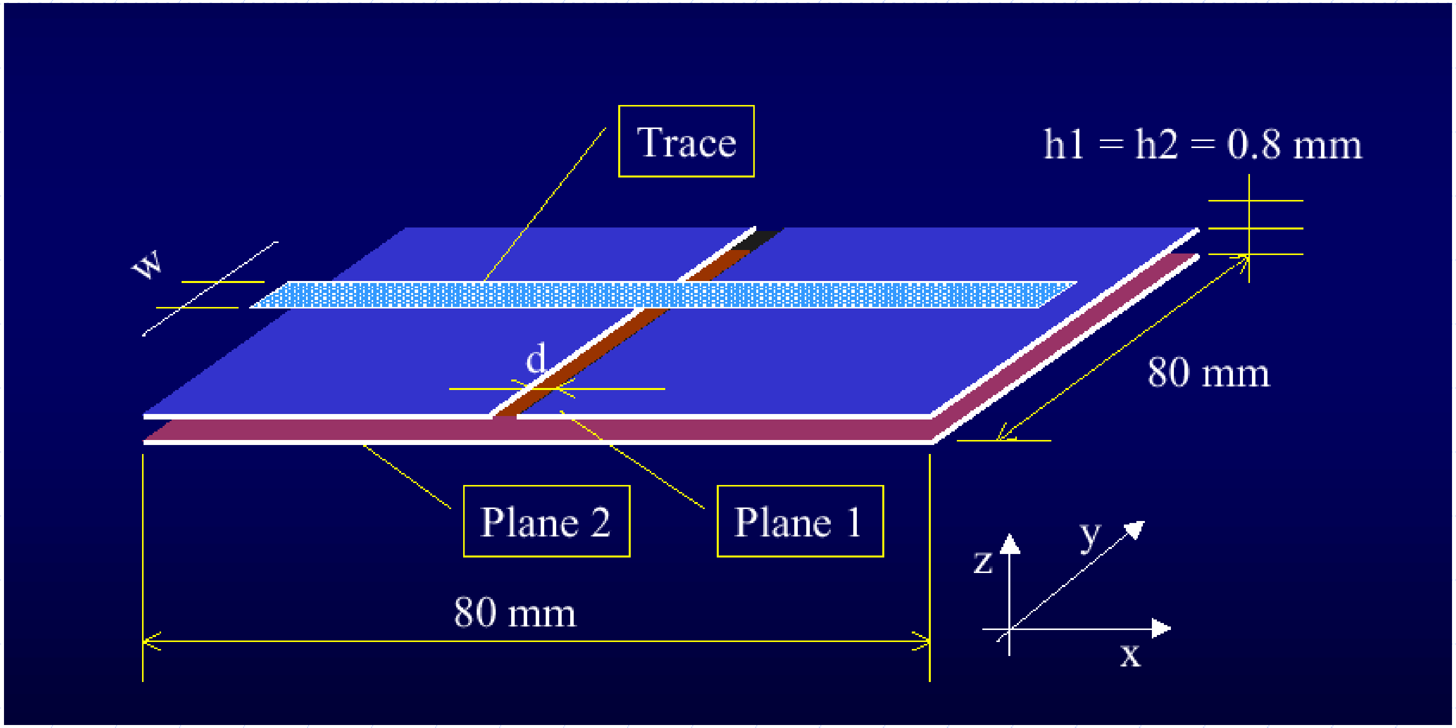
- AC shorting (stitching) the two separated planes with capacitors.



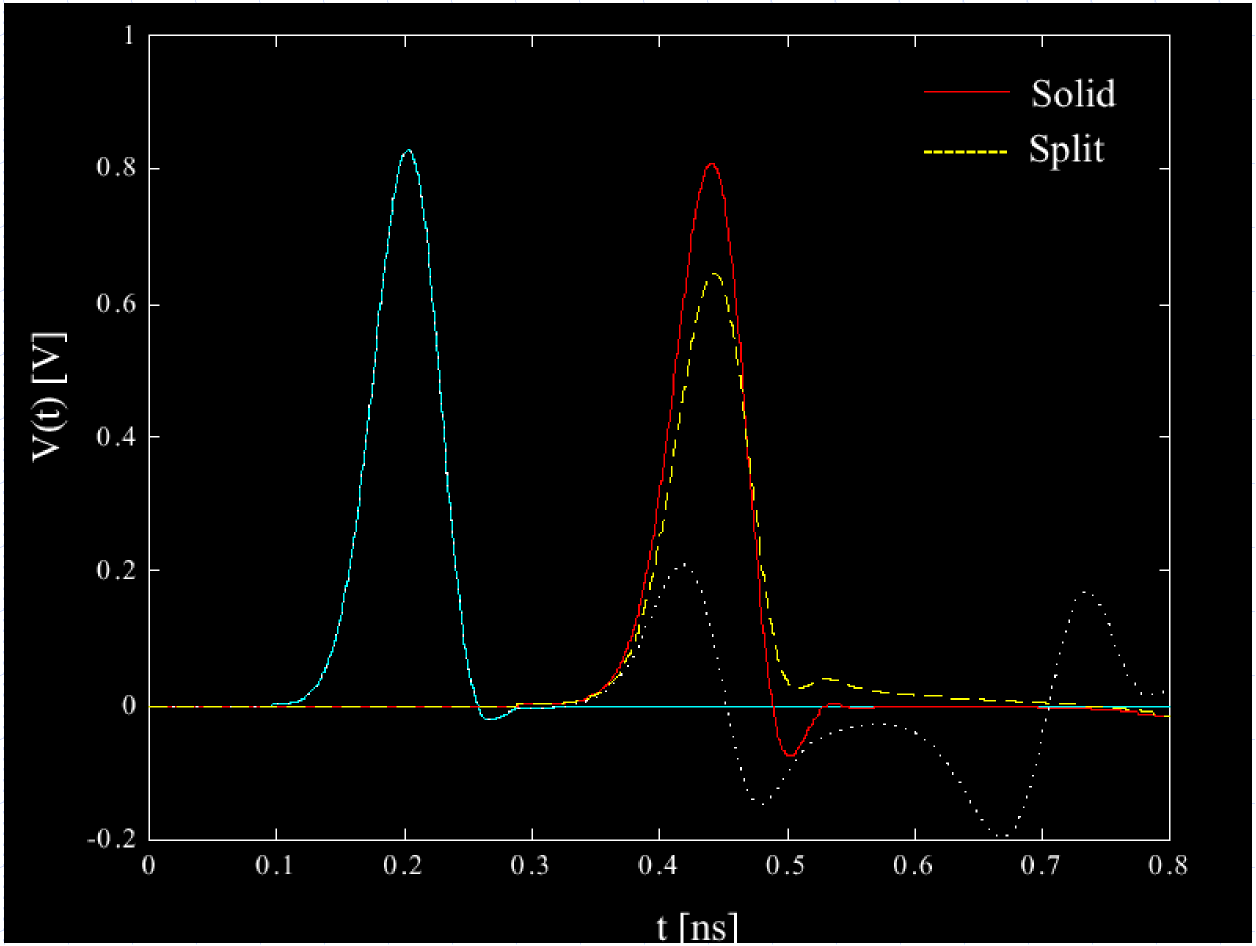
- Using differential lines to cross the split.



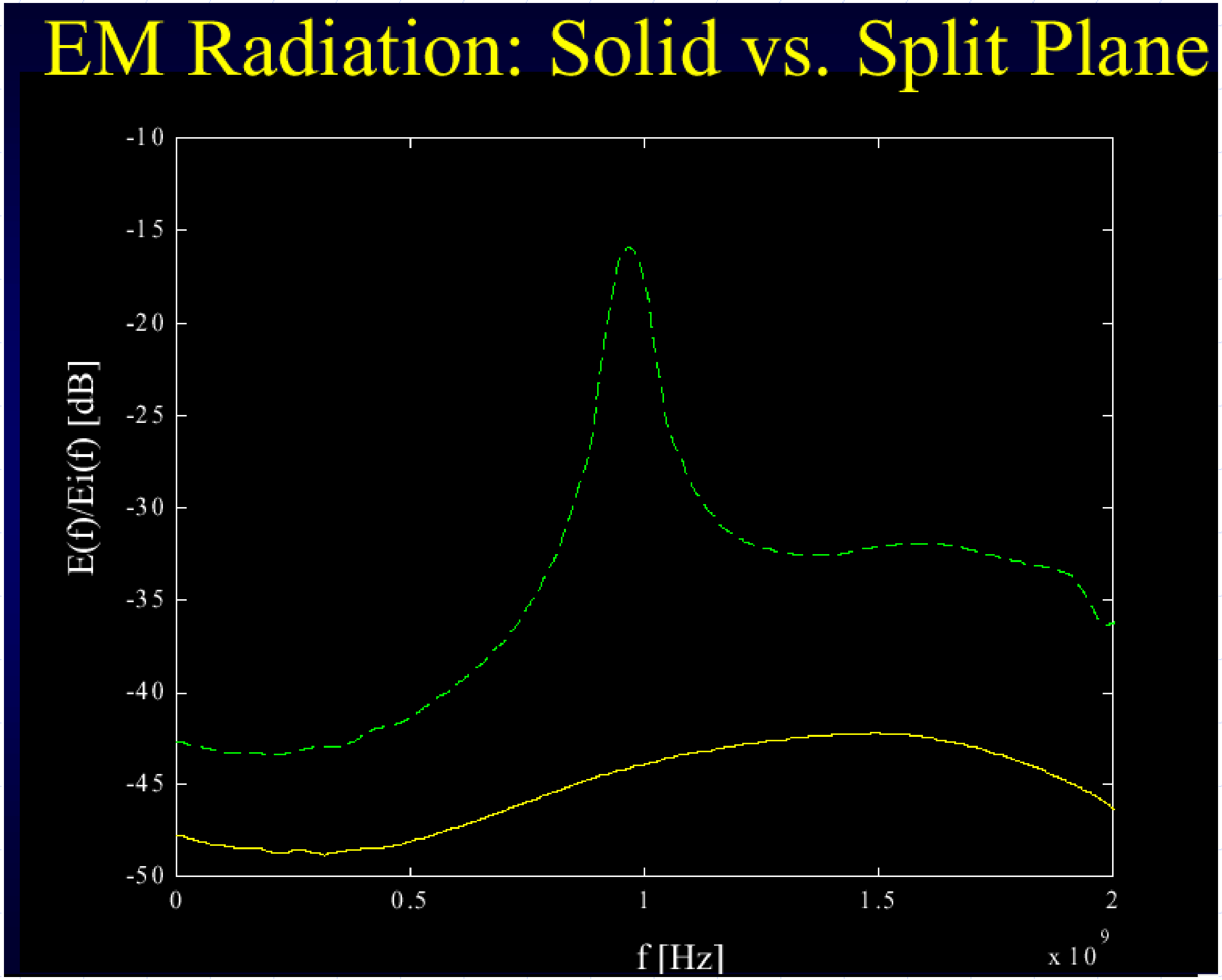
Example(II): Transmission line on non-ideal GND



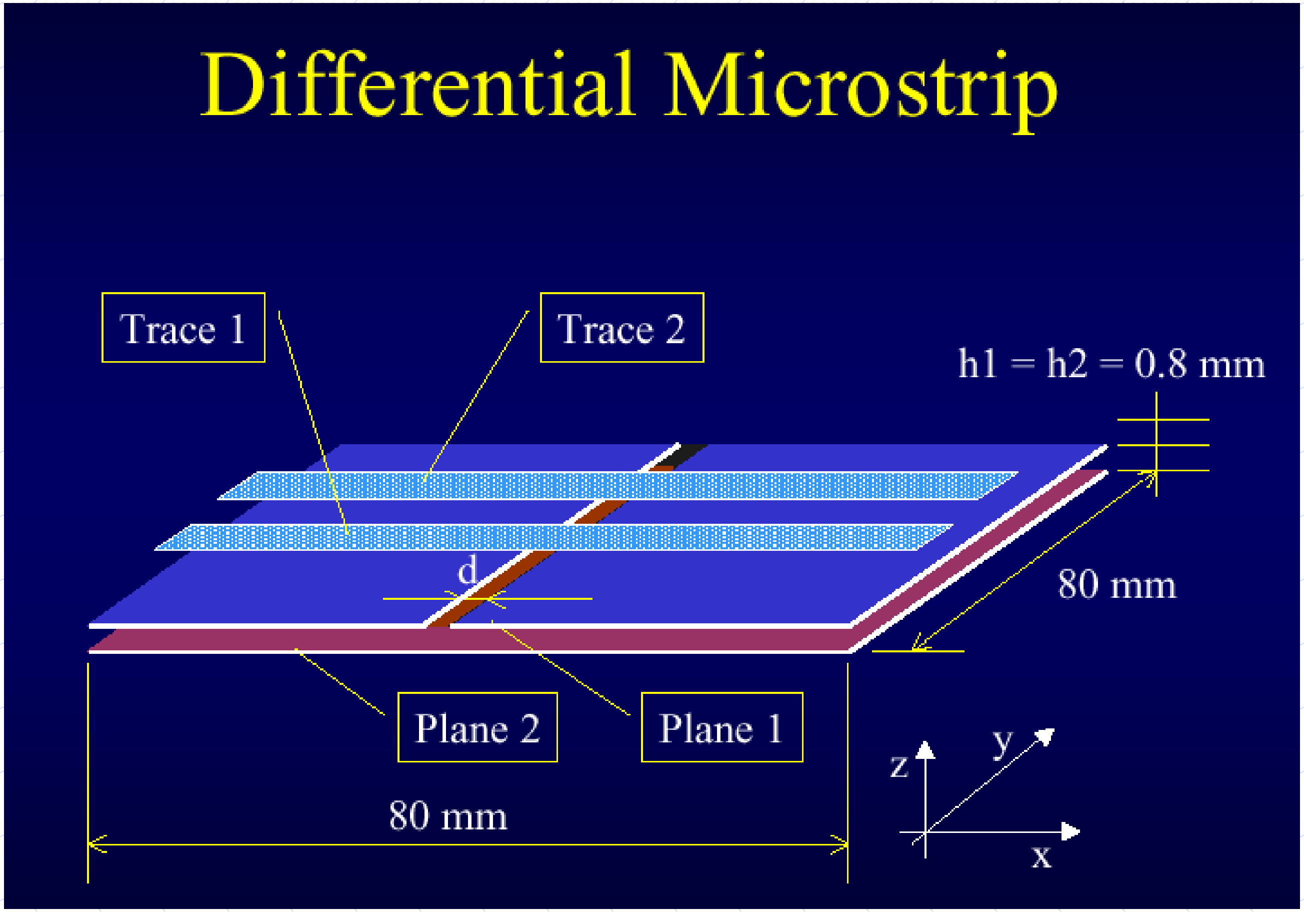
Example(II): Transmission line on non-ideal GND



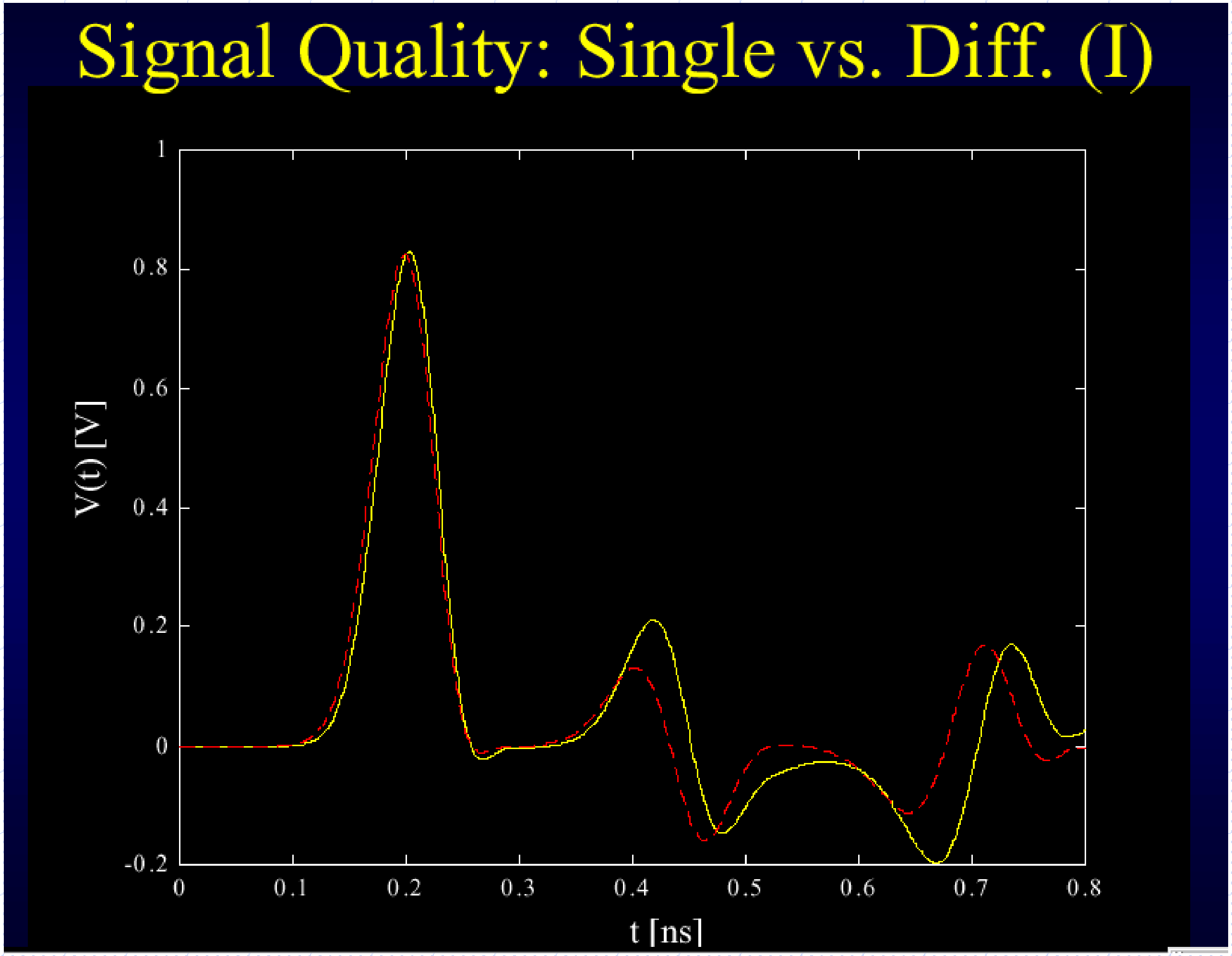
Example(II): Transmission line on non-ideal GND



Example(II): Transmission line on non-ideal GND

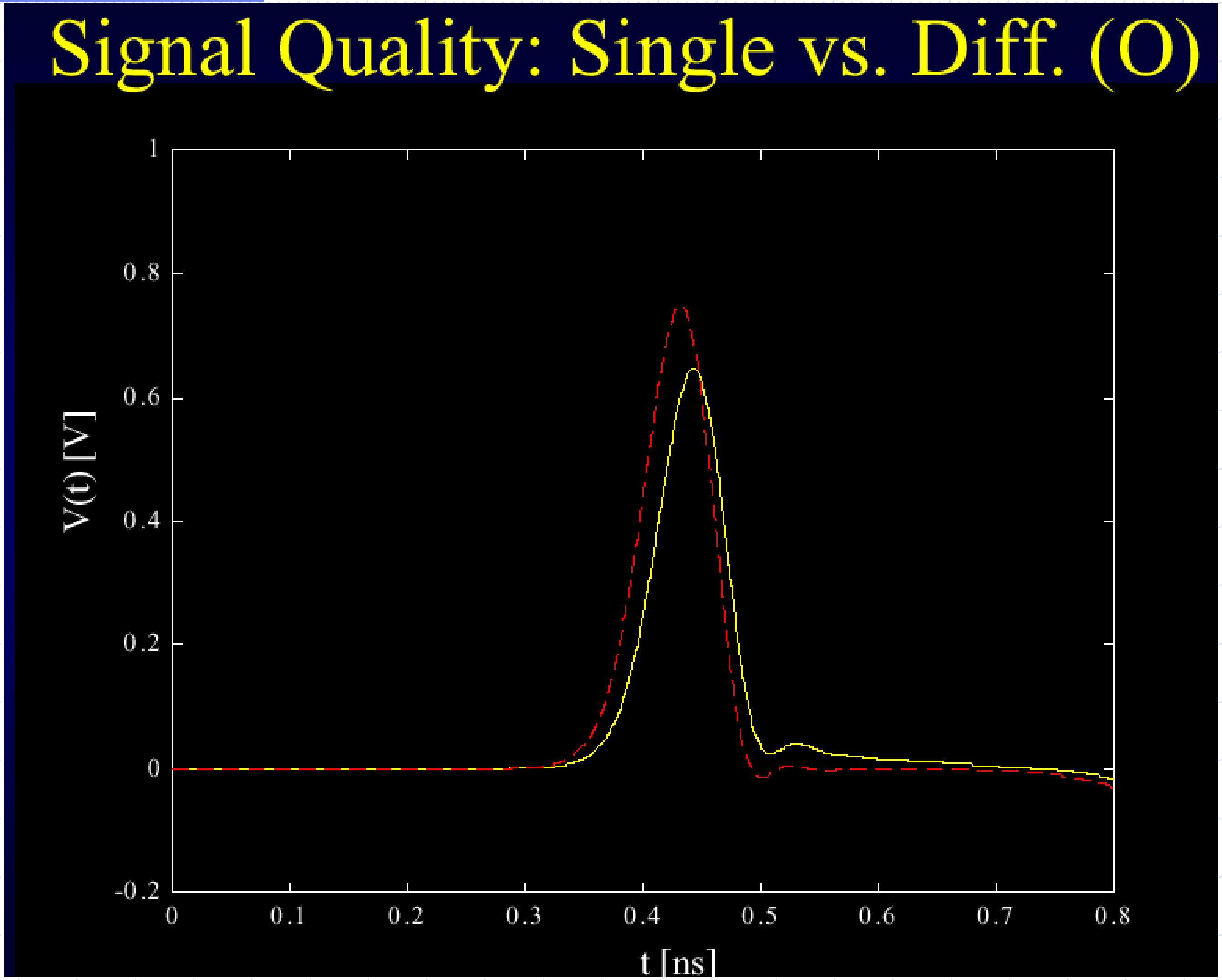


Input side



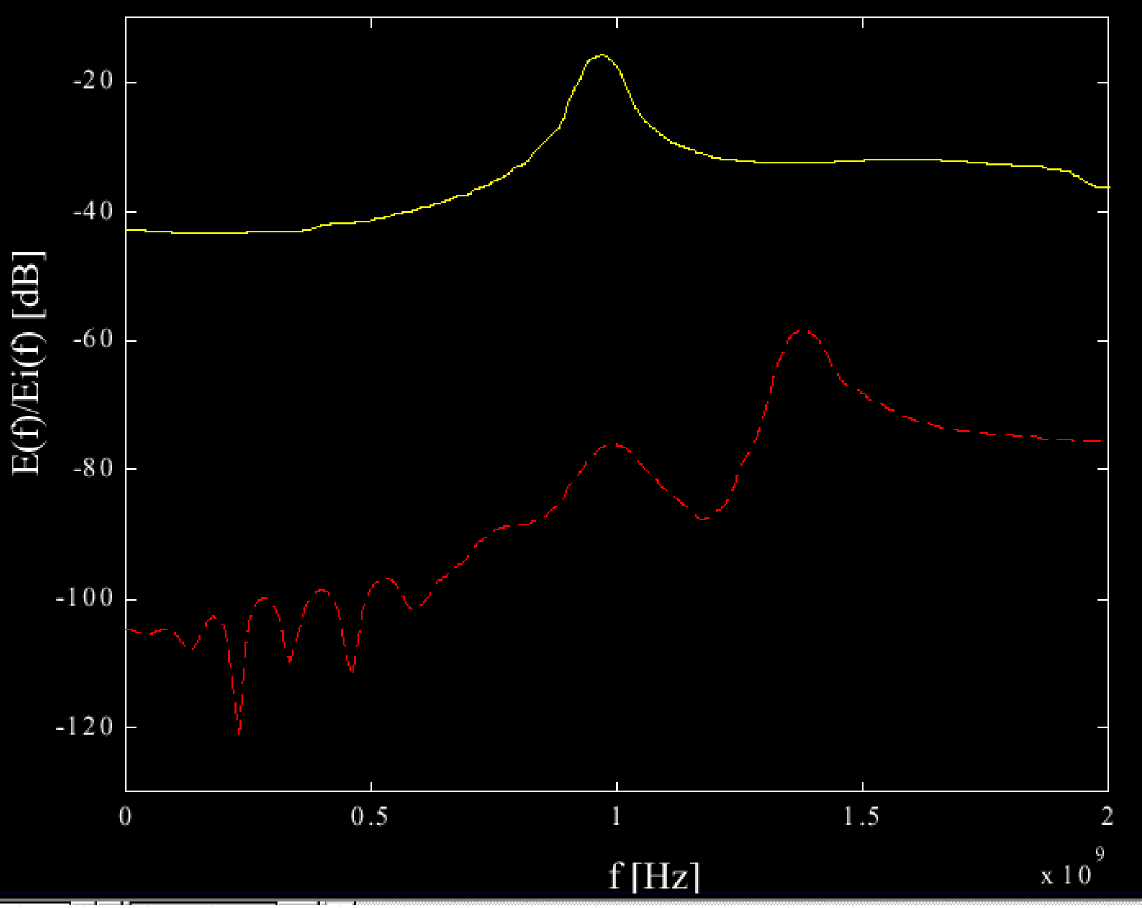
Signal Quality: Single vs. Diff. (I)
1
0.8
0.6
0.4
0.2
0
-0.2
V(t) [V]
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
t [ns]

Output side

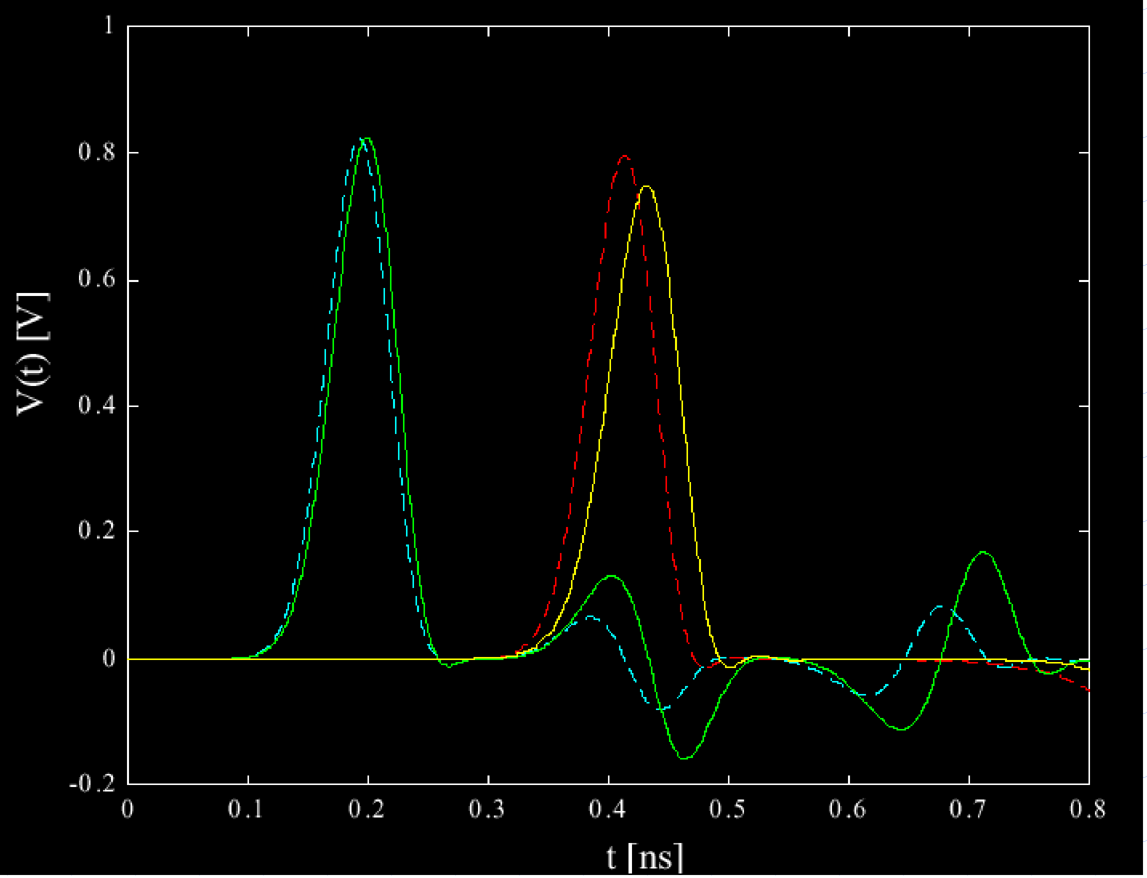


Signal Quality: Single vs. Diff. (O)
V(t) [V]
1
0.8
0.6
0.4
0.2
0
-0.2
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
t [ns]

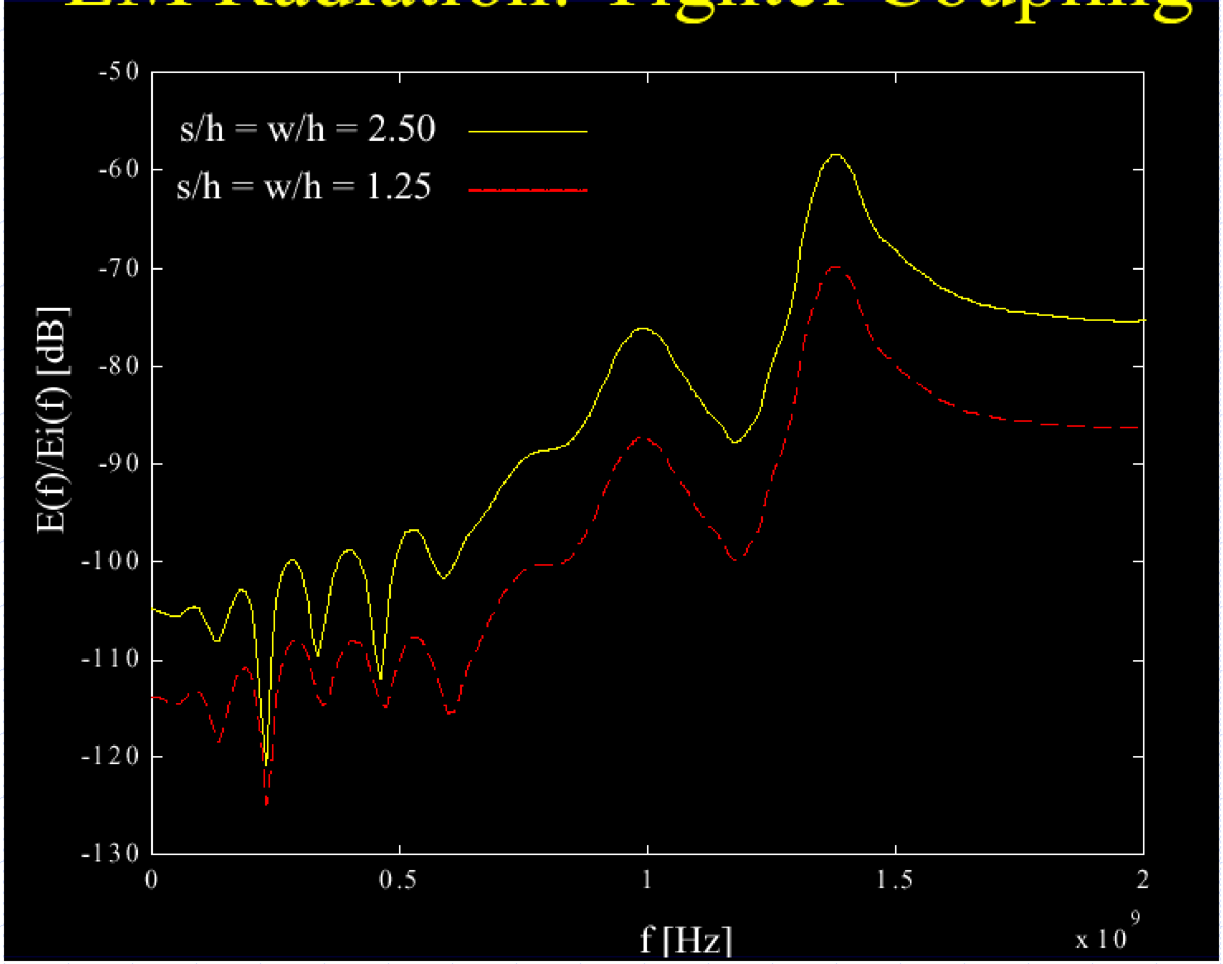
EM Radiation: Single vs. Diff.



Signal Quality: Tighter Coupling

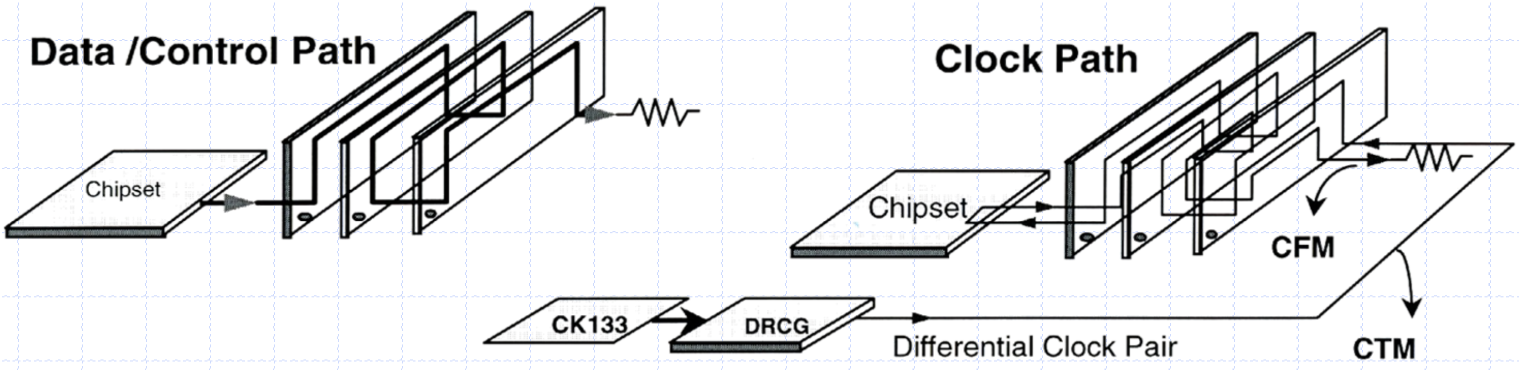


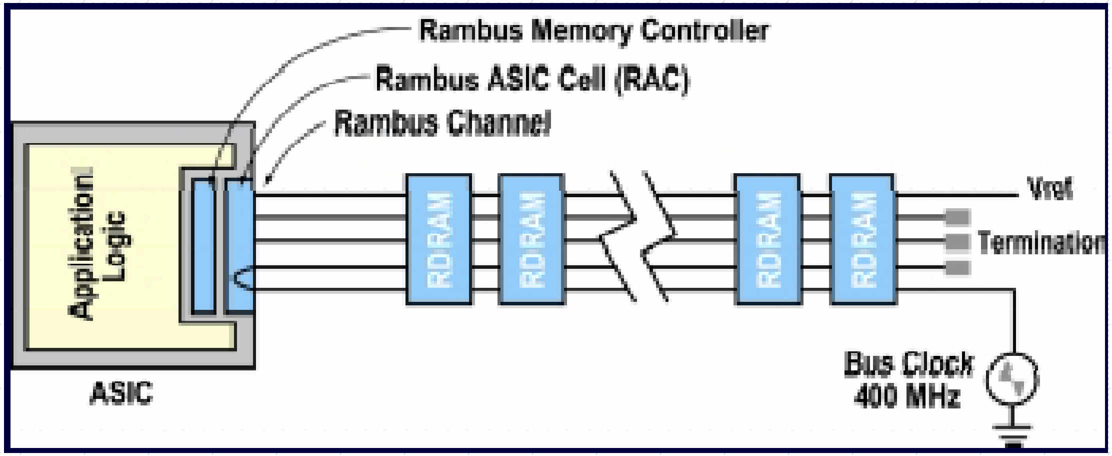
EM Radiation: Tighter Coupling



Example: Rambus RDRAM and RIMM Design

RDRAM Signal Routing





Example: Rambus RDRAM and RIMM Design

- Power:
  VDD = 2.5V, Vterm = 1.8V, Vref = 1.4V

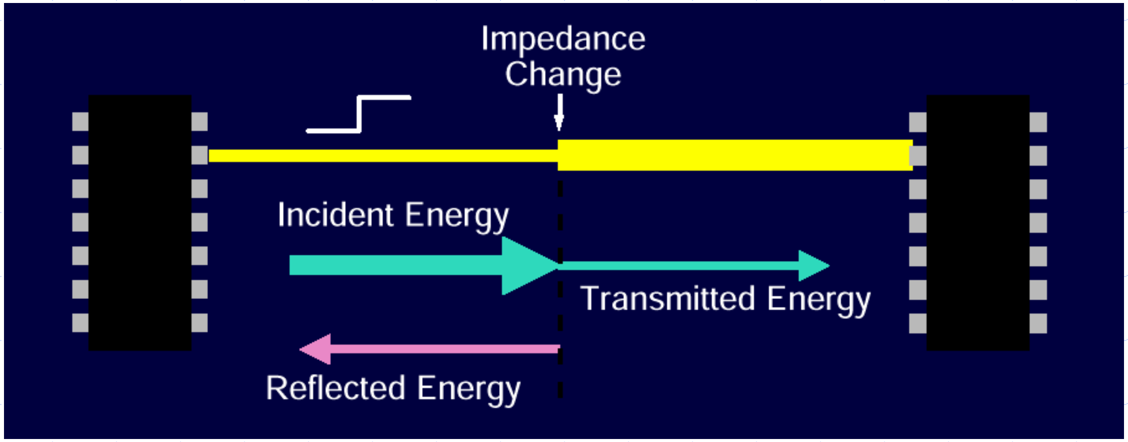
- Signal:
  0.8V Swing: Logic 0 -> 1.8V, Logic 1 -> 1.0V
  2x400MHz CLK: 1.25ns timing window, 200ps rise/fall time
  Timing Skew: only allow 150ps - 200ps

- Rambus channel architecture:
  (30 controlled impedance and matched transmission lines)

  - Two 9-bit data buses (DQA and DQB)
  - A 3-bit ROW bus
  - A 5-bit COL bus
  - CTM and CFM differential clock buses

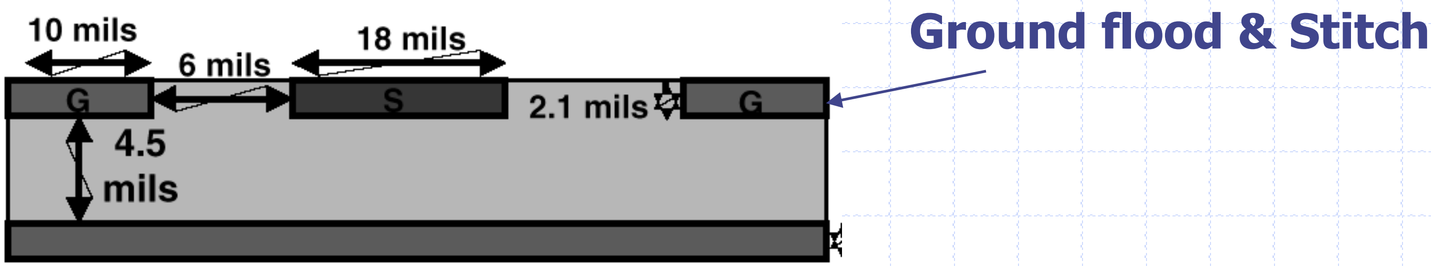
Example: Rambus RDRAM and RIMM Design

- RDRAM Channel is designed for 28 Ω +/- 10%
- Impedance mismatch causes signal reflections
- Reflections reduce voltage and timing margins
- PCB process variation -> Z_0 variation -> Channel error

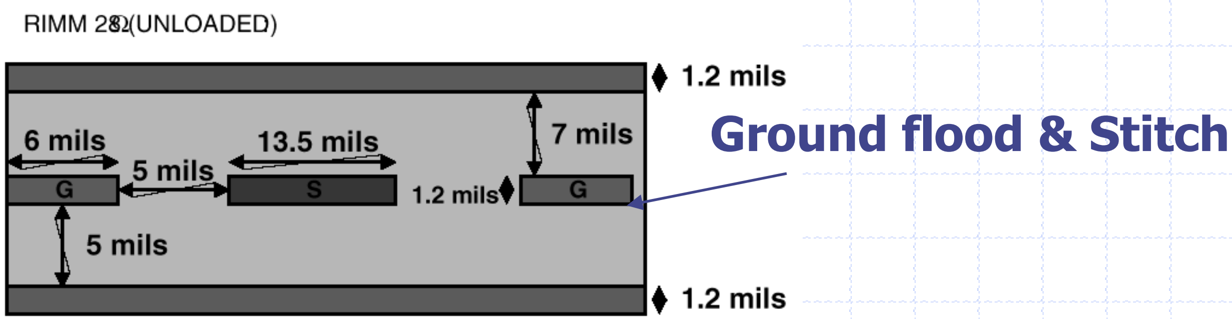


Example: Rambus RDRAM and RIMM Design

- Intel suggested coplanar structure



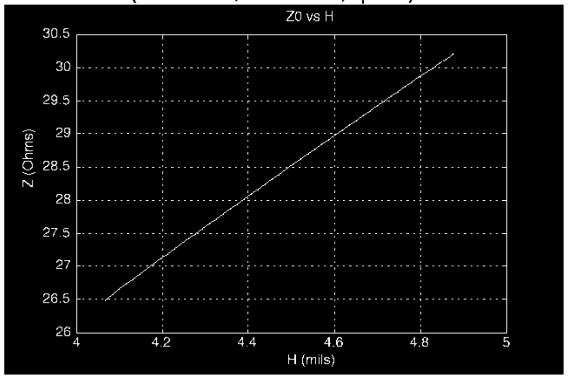
- Intel suggested strip structure



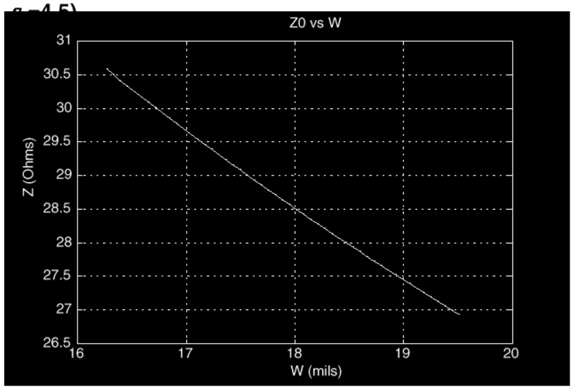
Example: Rambus RDRAM and RIMM Design

- PCB Parameter sensitivity:
  - H tolerance is hardest to control
  - W & T have less impact on Z_0

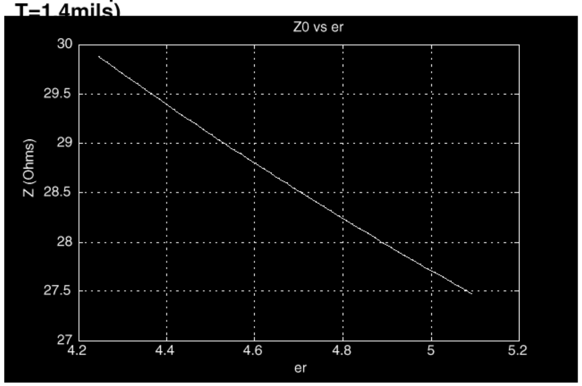
Z0 vs H (W=18mils, T=1.4mils, ε_r=4.5)



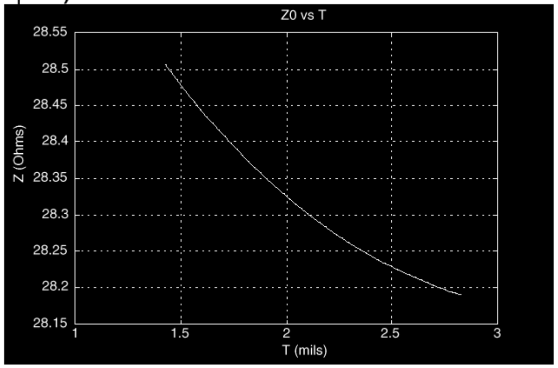
Z0 vs W (H=4.5mils, T=1.4mils, ε_r=4.5)



Z0 vs ε_r (H=4.5mils, W=18mils, T=1.4mils)

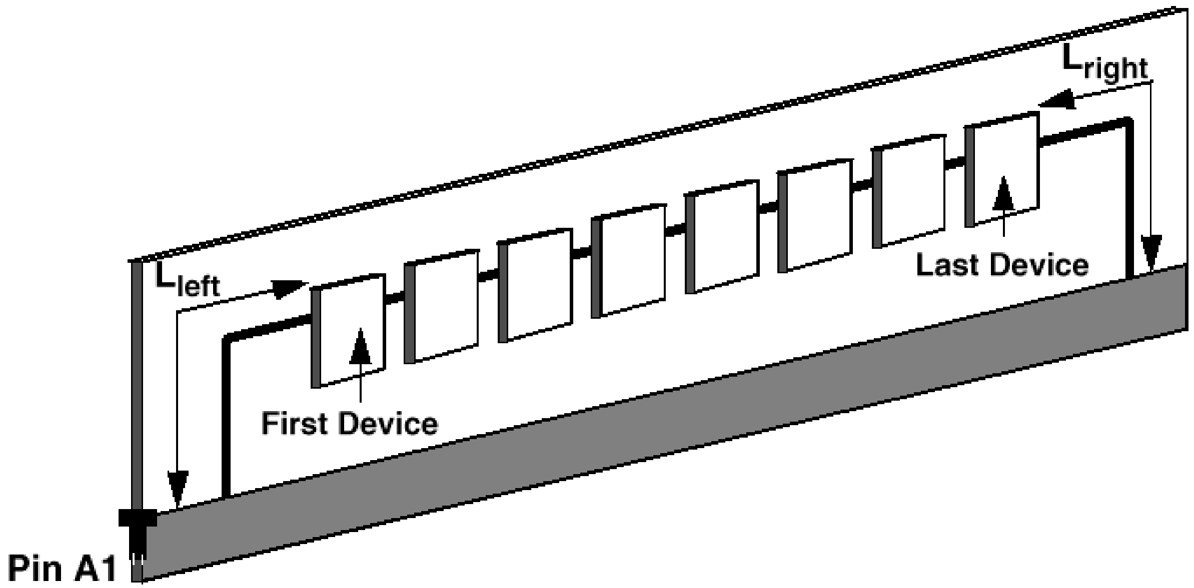


Z0 vs T (H=4.5mils, W=18mils, ε_r=4.5)



Example: Rambus RDRAM and RIMM Design

- How to design Rambus channel in *RIMM Module* with uniform Z_0 = 28 ohm ??
- How to design Rambus channel in *RIMM Module* with propagation delay variation in +/- 20ps ??



Example: Rambus RDRAM and RIMM Design

Impedance Control: (Why?)

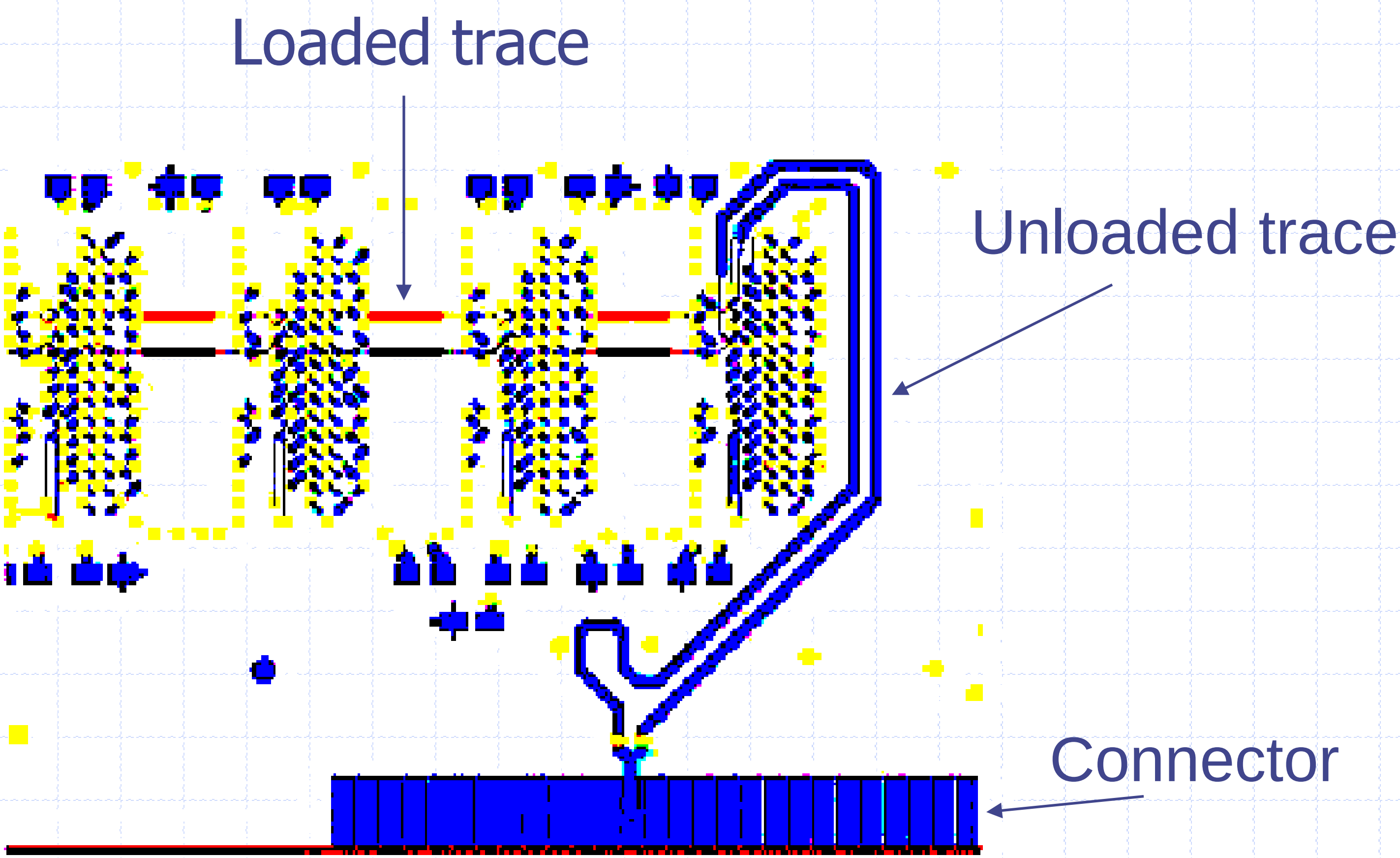
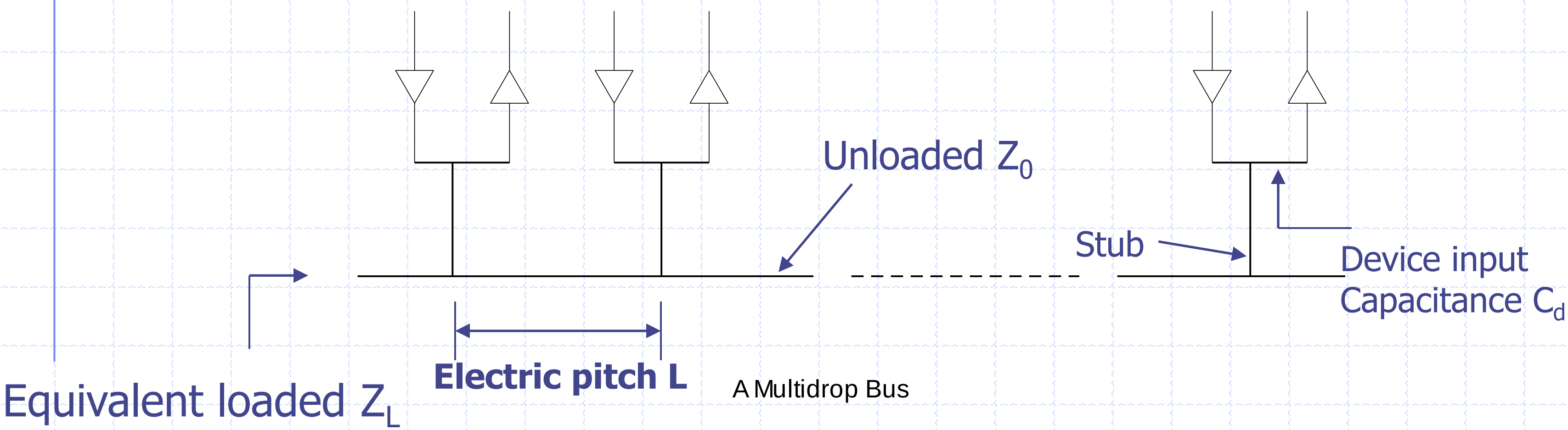


Figure 5-12: High-Speed CMOS Signal Routing

Example: Rambus RDRAM and RIMM Design

Multi-drop Buses



$$Z_L = \sqrt{\frac{L_0}{C_T}} = \sqrt{\frac{L_0}{\frac{C_L}{L} + \frac{L_0}{Z_0^{\,2}}}} = 28\Omega \text{ (for Rambus design)}$$

where C_T is the per-unit-length equivalent capacitance at length L, including the loading capacitance and the unloaded trace capacitance

C_L is the loading capacitance including the device input capacitance C_d, the stub trace capacitance, and the via effect.

Example: Rambus RDRAM and RIMM Design

In typical RIMM module design

stub — via — Device input capacitance

If $C_L = 0.2\text{pF} + 0.1\text{pF} + 2.2\text{pF}$, and

If you design unloaded trace $Z_0 = 56\Omega$

the electric pitch L = 7.06mm to reach loaded $Z_L = 28\Omega$

$$\because L_0 = Z_0 \tau = 56\Omega \times 6.77 \text{ psec / mm} = 379 \text{ pH / mm} = 9.5 \text{ pH / mil}$$

$$C_T = \frac{C_L}{L} + \frac{L_0}{Z_0^{\ 2}} = \frac{2.5pF}{7.06mm} + \frac{379 \text{ pH / mm}}{56\Omega^2} = 0.475 \text{ pF / mm}$$

$$\therefore Z_L = \sqrt{\frac{L_0}{C_T}} = 28.3\Omega$$

Example: Rambus RDRAM and RIMM Design

- Modulation trace

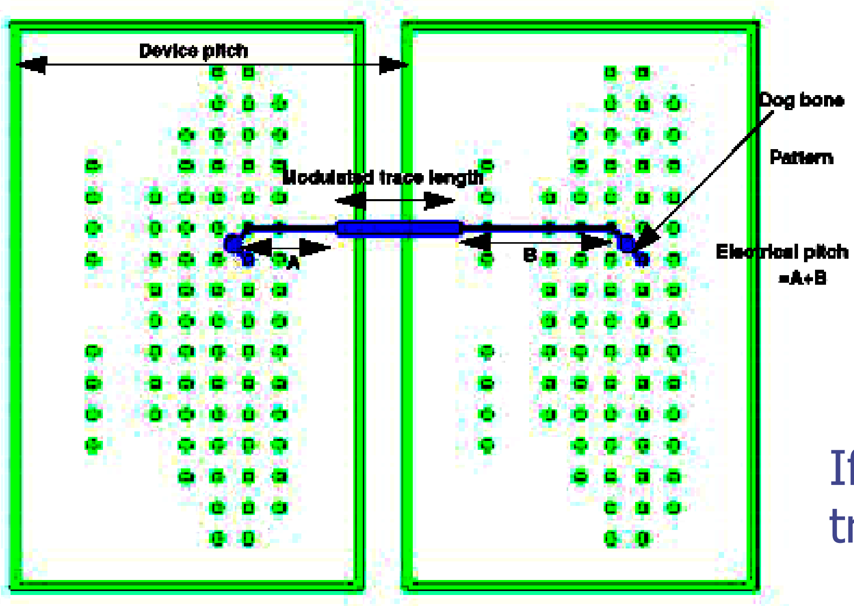


Figure 5-5: 8 Device Single-Sided Edge-Bonded Module Device and Electrical Pitch

Device pitch = Device height + Device space

Electrical pitch L is designed as

$$L = \frac{C_L Z_L^{2}}{\frac{\tau}{Z_0}(Z_0^{2} - Z_L^{2})}$$

If device pitch > electric pitch, modulation trace of 28ohm should be used.

Modulation trace length
= Device pitch – Electric pitch

Example: Rambus RDRAM and RIMM Design

- Effect of PCB parameter variations on three key module electric characteristics

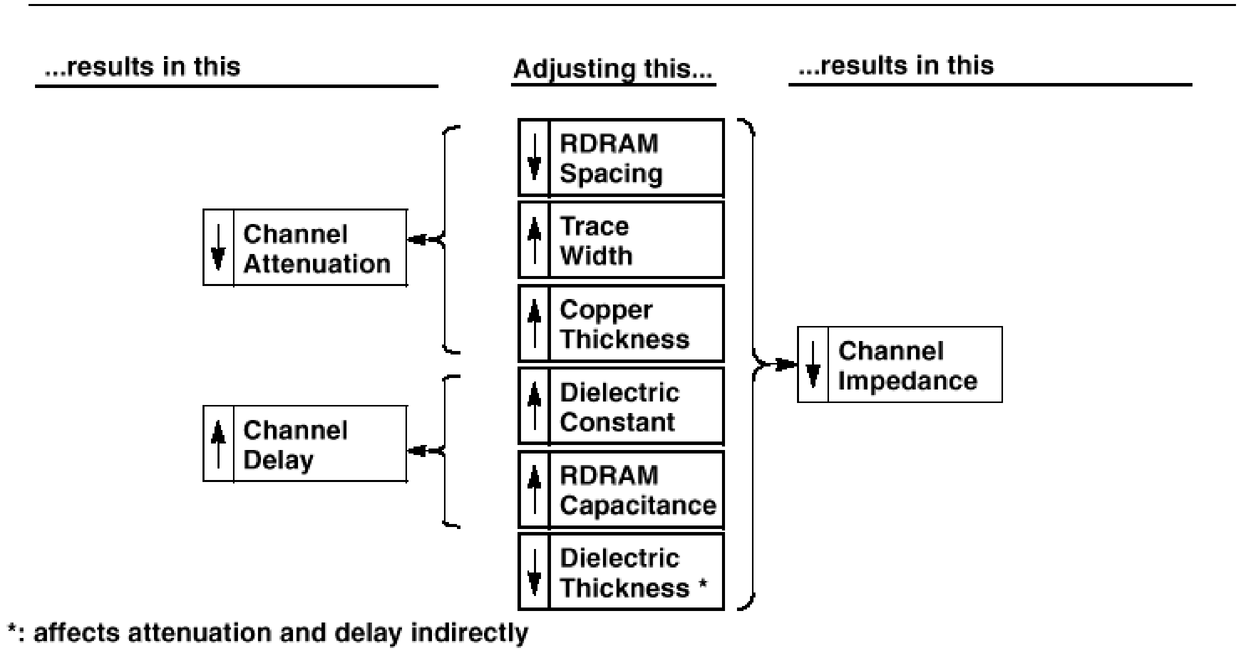


Figure 2-3: PCB Design Parameter Relationships

Example: Rambus RDRAM and RIMM Design

- Controlling propagation delay:
  - *Bend compensation*
  - *Via Compensation*
  - *Connector compensation*

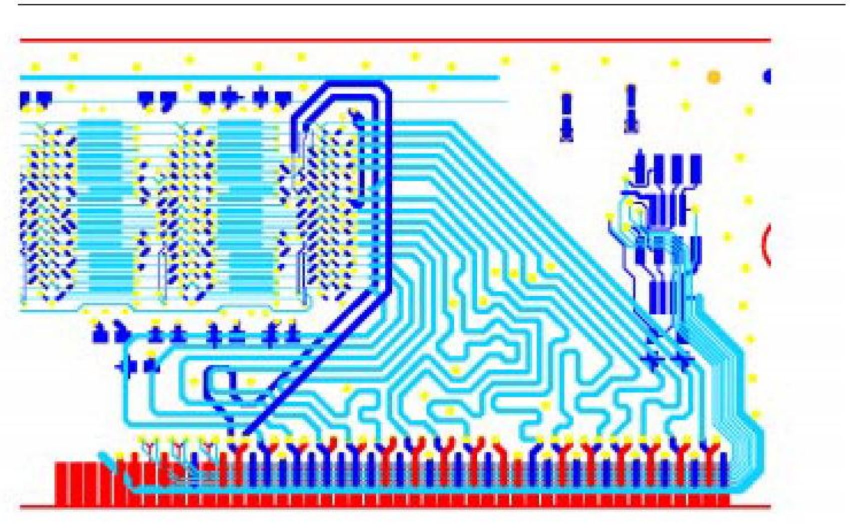


Figure 5-11: Delay Matching (Right Side)

Bend Compensation

- Rule of thumb: 0.3ps faster delay of every bend
- Solving strategies:
  1. Using same numbers of bends for those critical traces(difficult)
  2. Compensate each bend by a 0.3ps delay line.

Example: Rambus RDRAM and RIMM Design

Via Compensation (delay)

For a 8 layers PCB, a via with 50mil length can be modeled as (L, C) = (0.485**nH**, 0.385**pF**).

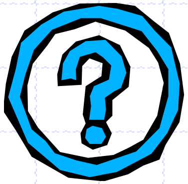
$$\therefore \text{Delay } T_0 = \sqrt{LC} = 13.7 \text{ psec}$$

$$\text{Impedance } Z_0 = \frac{1}{\sqrt{\text{LC}}} \approx 38\Omega \longleftarrow \text{Inductive}$$

Rule of thumb: delay of a specific via depth can be calculated by scaling the inductance value which is proportional to via length.

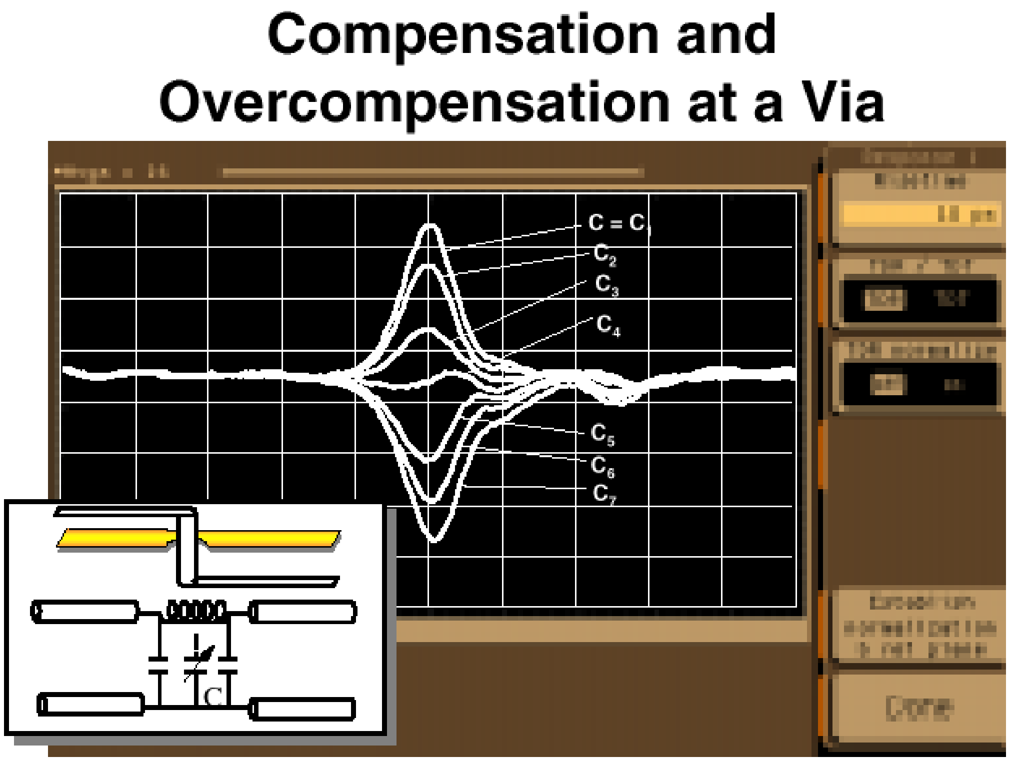
$$\therefore \text{30mil via has delay } \approx 13.7 \times \sqrt{\frac{\text{30mil}}{\text{50mil}}} = 10.6\,p\,\text{sec}$$

This delay difference can be compensated by adding a 1.566mm to the unloaded trace (56Ω)



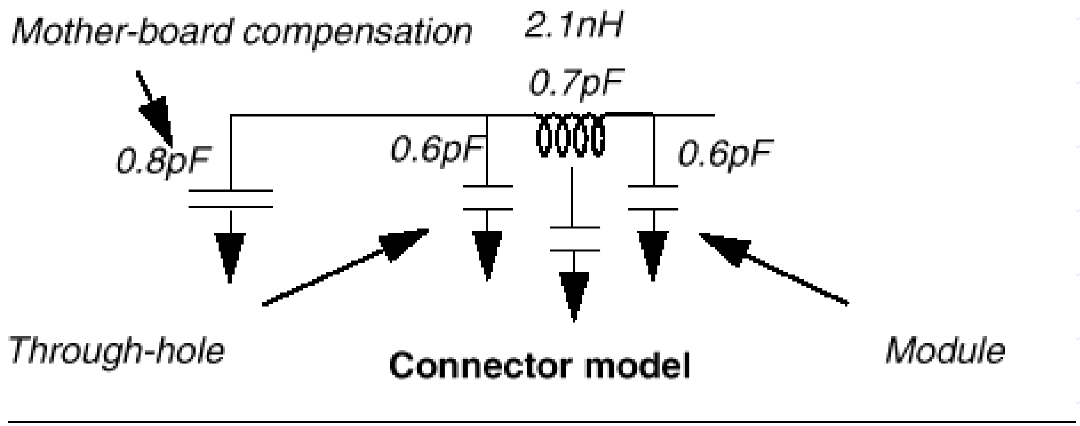
Example: Rambus RDRAM and RIMM Design

Via Compensation (impedance)



Example: Rambus RDRAM and RIMM Design

Connector Compensation



Cpin = 0.7pF, Cvia = 0.6pF, Cpad = 0.6pF, Cmb=0.8pF => Ctotal = 2.7pF

Lpin = 2.1nH

$$Z = \sqrt{(Lpin)/(Ctotal)} = 27.9\Omega$$

Example: EMI resulting from a trace near a PCB edge

Experiment setup and trace design

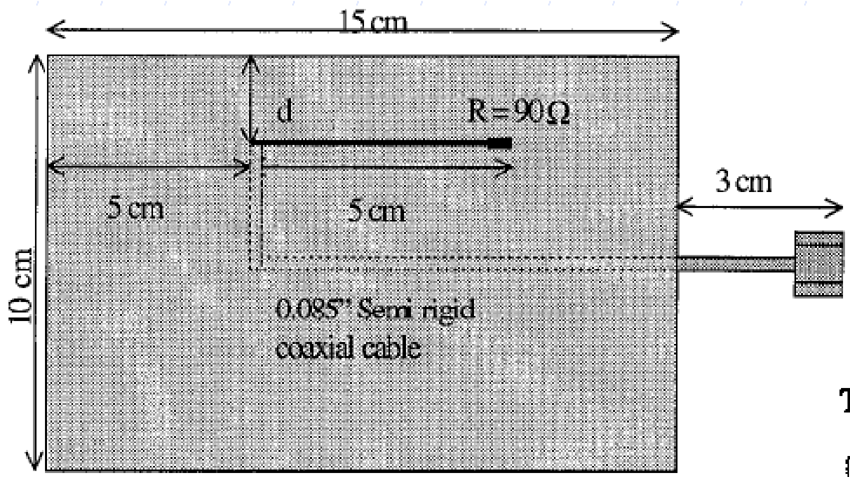


Figure 1: Geometry of PCB layout.

Table 1. Comparison of height above PCB reference plane and trace proximity to board edge (d).

Height (mils)	d (mils)	d/h	Termination
45	25	0.55	90 Ω
45	75	1.67	90 Ω
45	275	6.11	90 Ω
45	575	12.8	90 Ω
45	1956 (centered)	43.5	90 Ω
90	1956 (centered)	21.7	116 Ω
22	1956 (centered)	88.9	60 Ω
22	25	1.14	60 Ω

Example: EMI resulting from a trace near a PCB edge

Measurement Setup

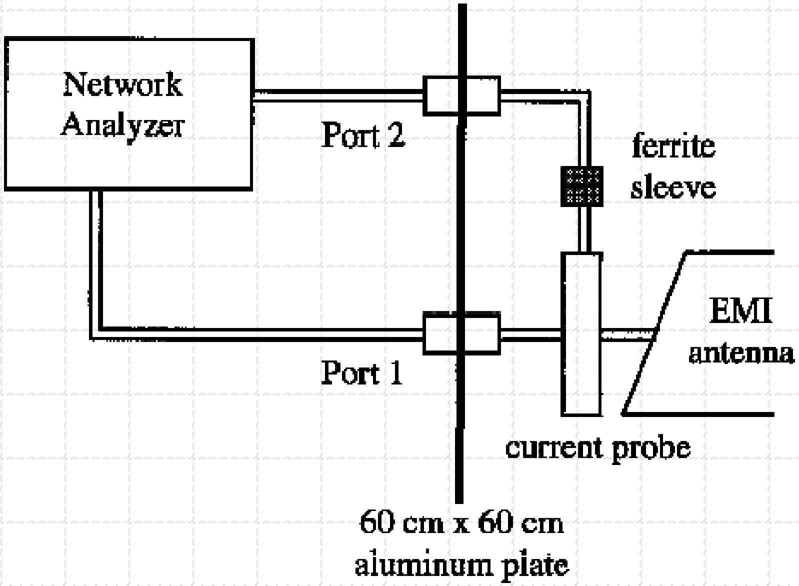


Figure 2: Test setup for measuring the $|S_{21}|$ with a current probe.

Example: EMI resulting from a trace near a PCB edge

EMI caused by Common-mode current : magnetic coupling
Measured by current probe

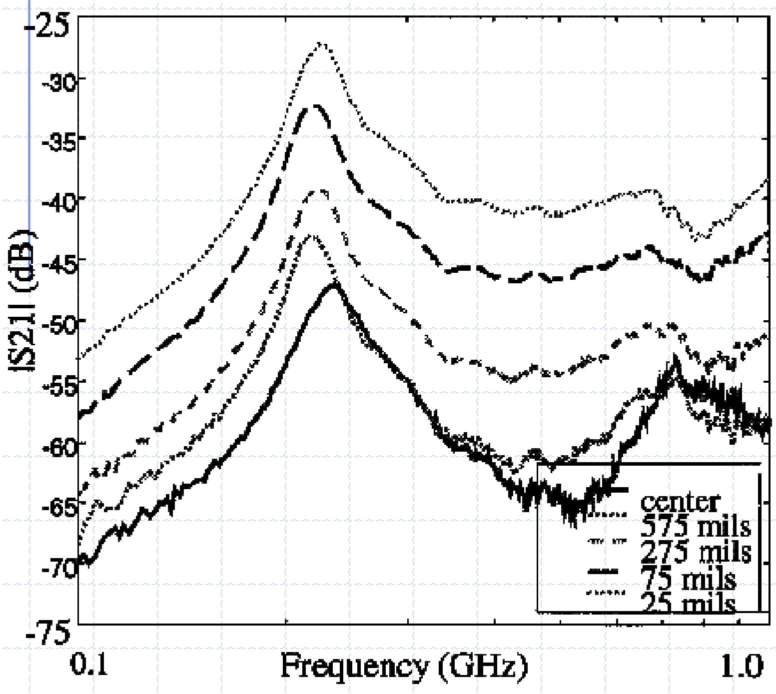


Figure 3: $|S_{21}|$ measurements with a current probe.

Table 2. Increase in $|S_{21}|$ as the trace nears the PCB edge. The reference is a centered trace.

Distance from Edge (d)	$\Delta\|S_{21}\|$ (dB)
25 mils.	17.6
75 mils.	13.1
275 mils.	6.61
475 mils.	3.33

Example: EMI resulting from a trace near a PCB edge

EMI measured by the monopole : E field

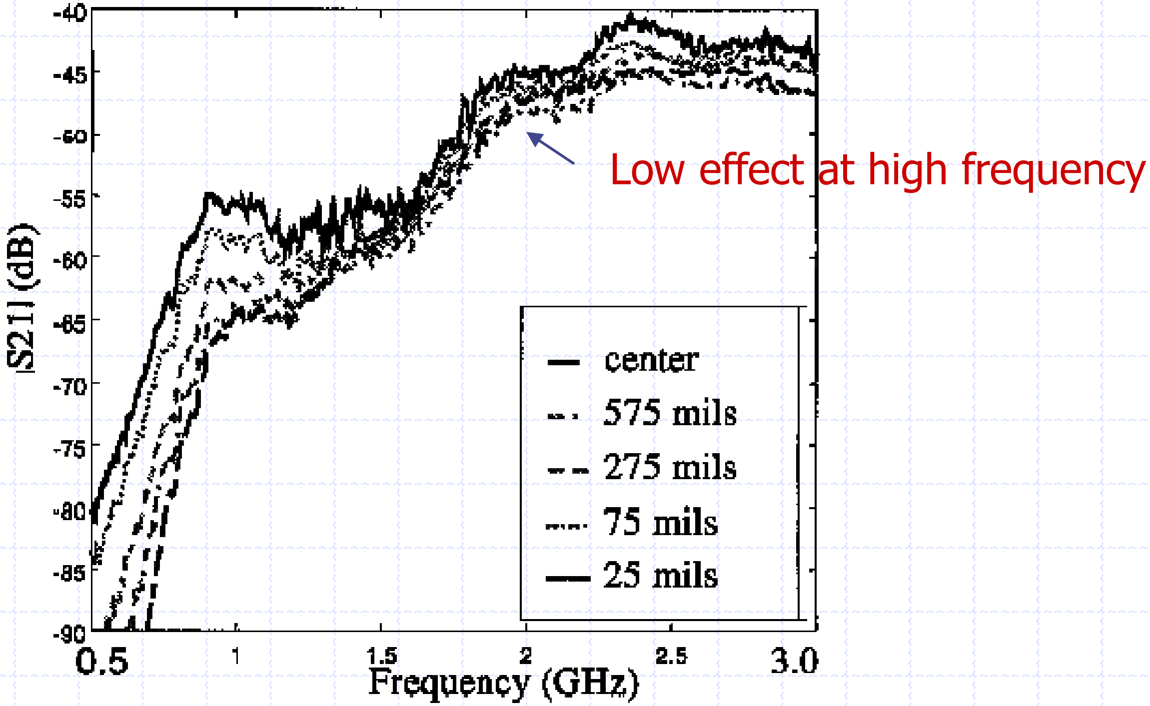


Figure 4: $|S_{21}|$ measurements using a 3 cm monopole probe.

Example: EMI resulting from a trace near a PCB edge

Trace height effect on EMI

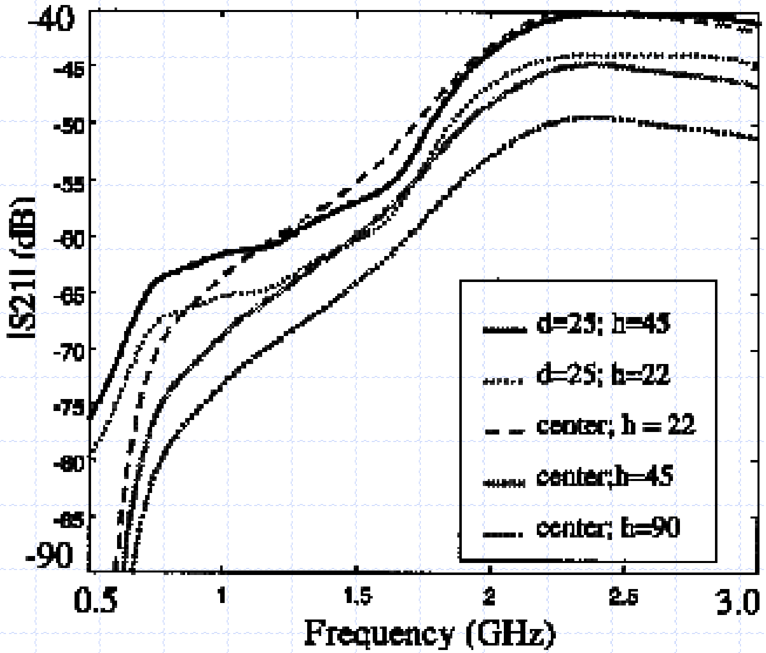


Figure 8: Comparison of the near-electric field radiation for different trace heights above the reference plane for a centered trace, and trace 25 mils from edge.

Reference

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