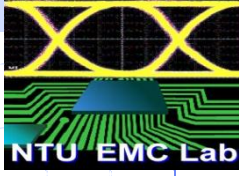

Transient Response of Transmission Lines and TDR/TDT

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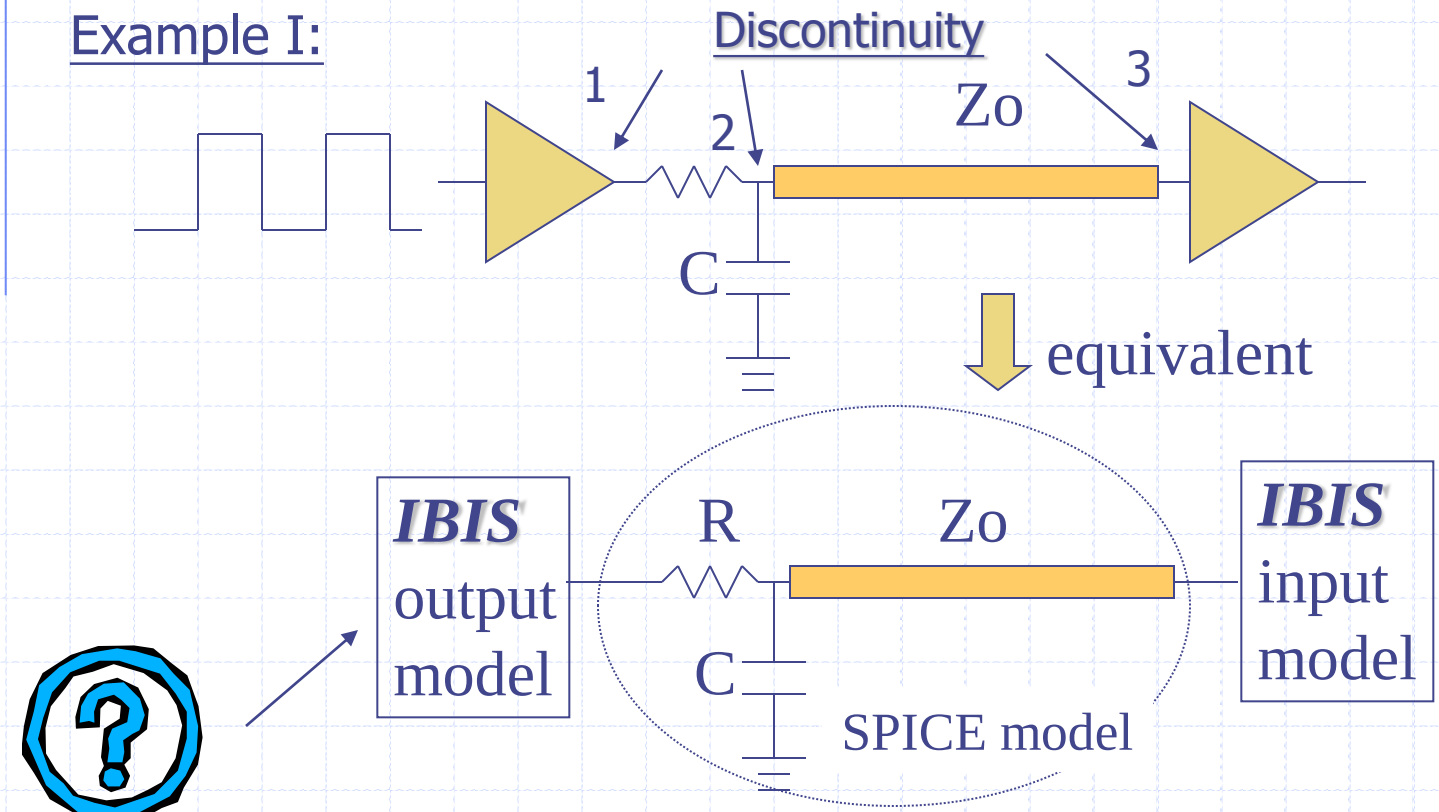
Outlines

- Why do we learn the transient response of transmission line ?
  - Example I
  - Example II
- Reflection at Discontinuity
  - Resistive discontinuity
  - Reactive discontinuity
- Termination
- TDR / TDT fundamentals

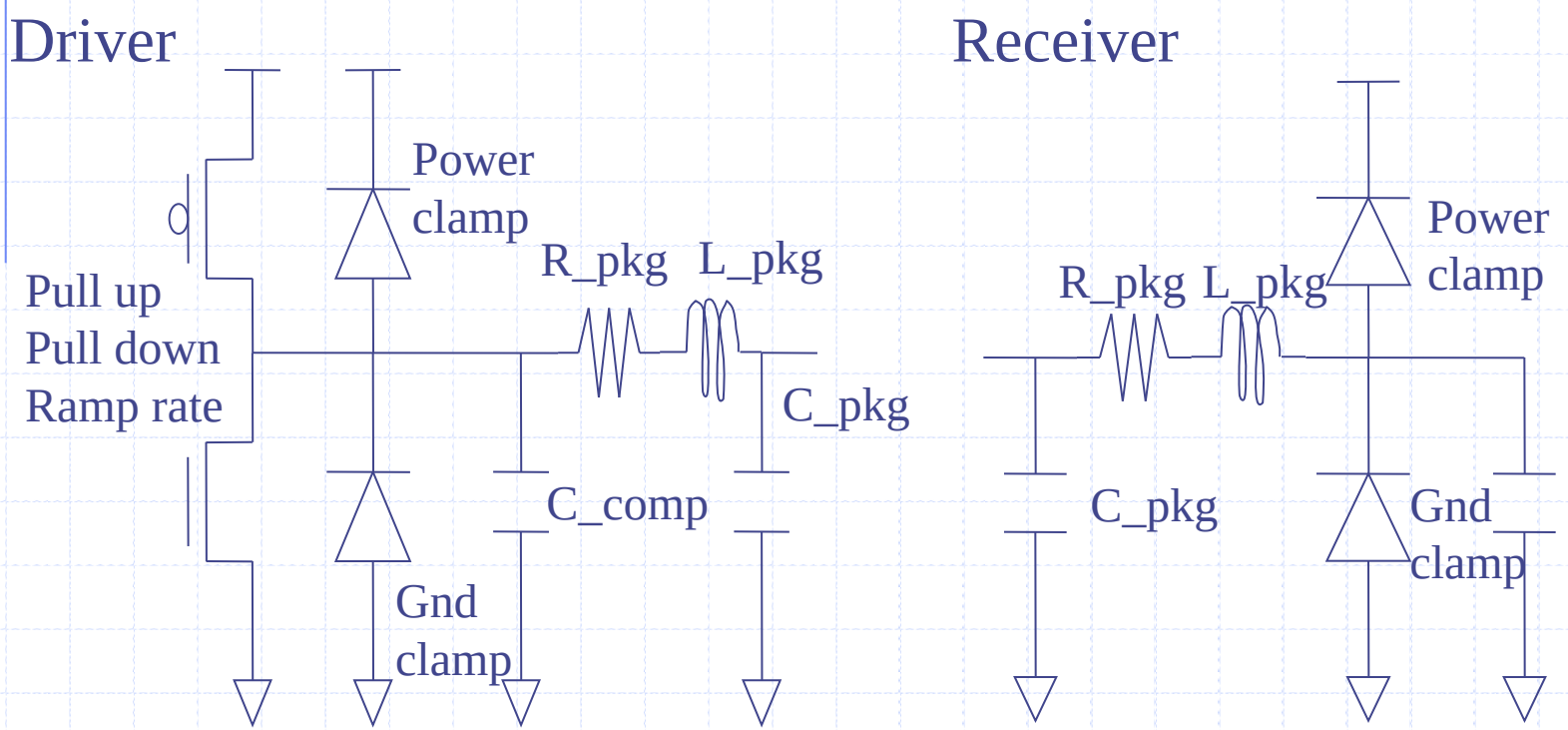
Why do we learn transient response ? (Example: I)

- Discontinuity can not be avoided in the high speed digital circuits.



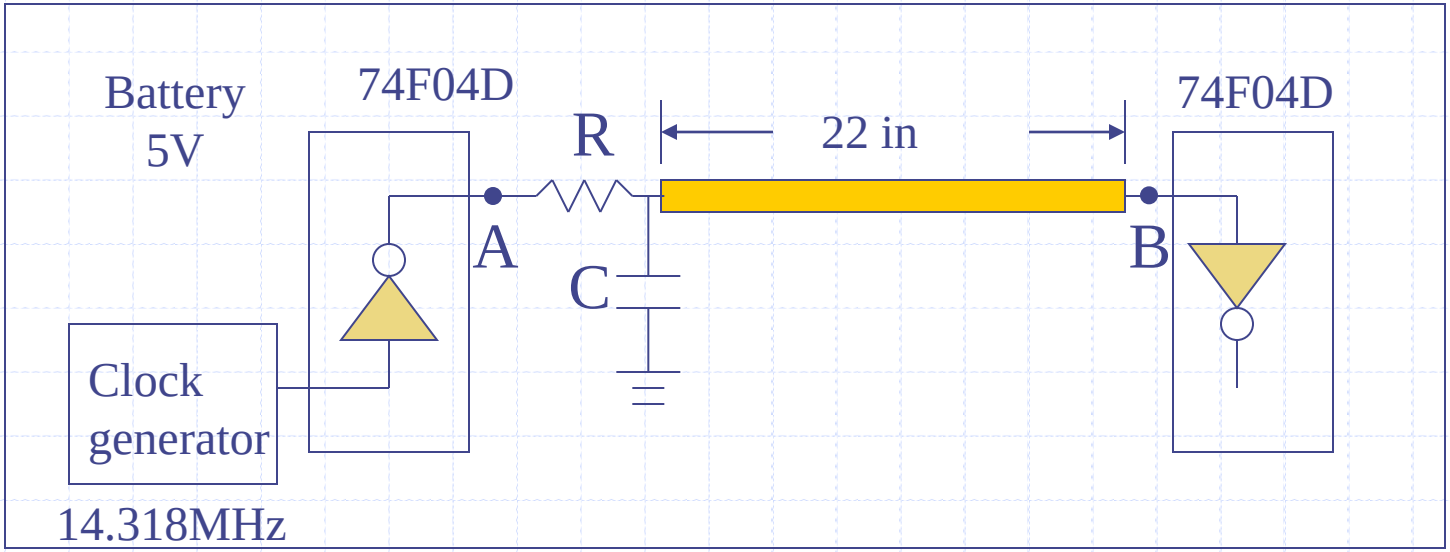
Why do we learn transient response ? (IBIS Model)

- IBIS (I/O Buffer Information Spec.) Model:



Why do we learn transient response ? (Example: I)

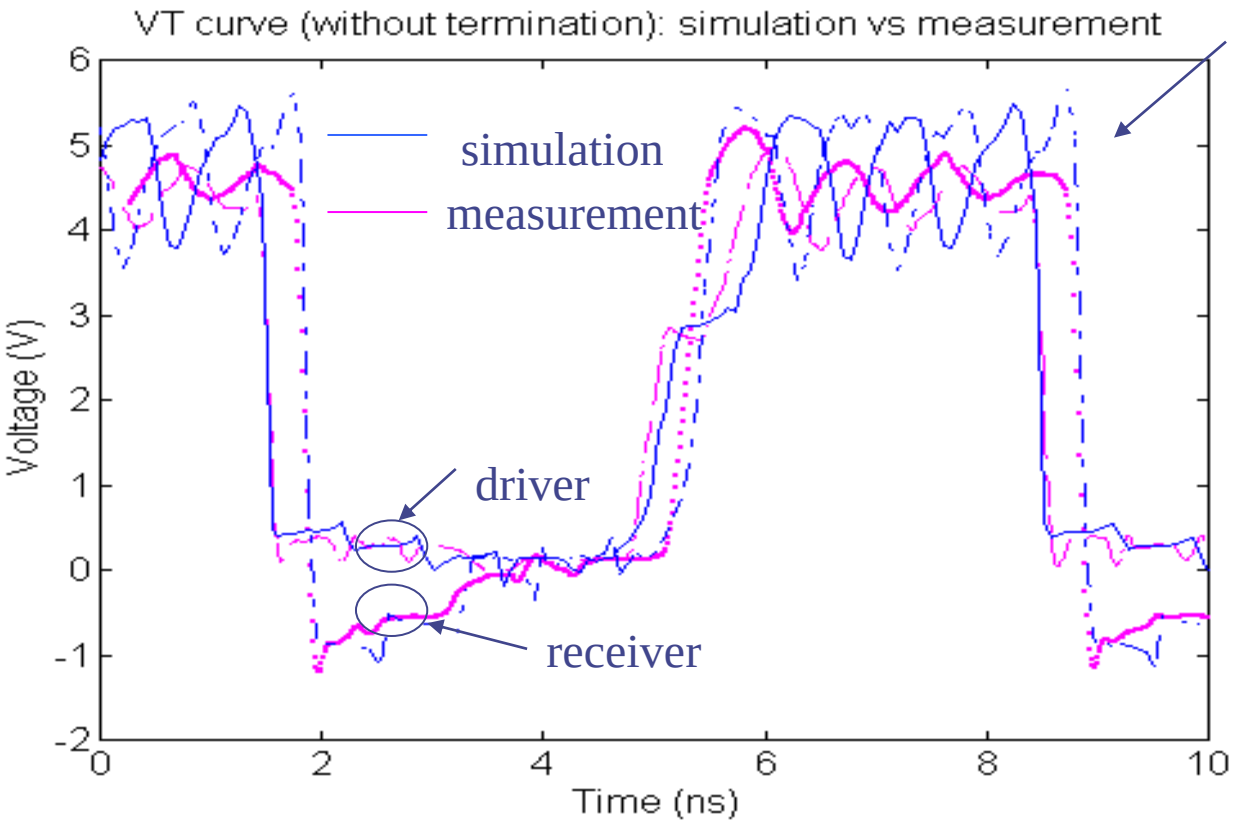
- Experimental setup
  - PCB: 25*3in (L*W), h=0.059in, εr=4.5



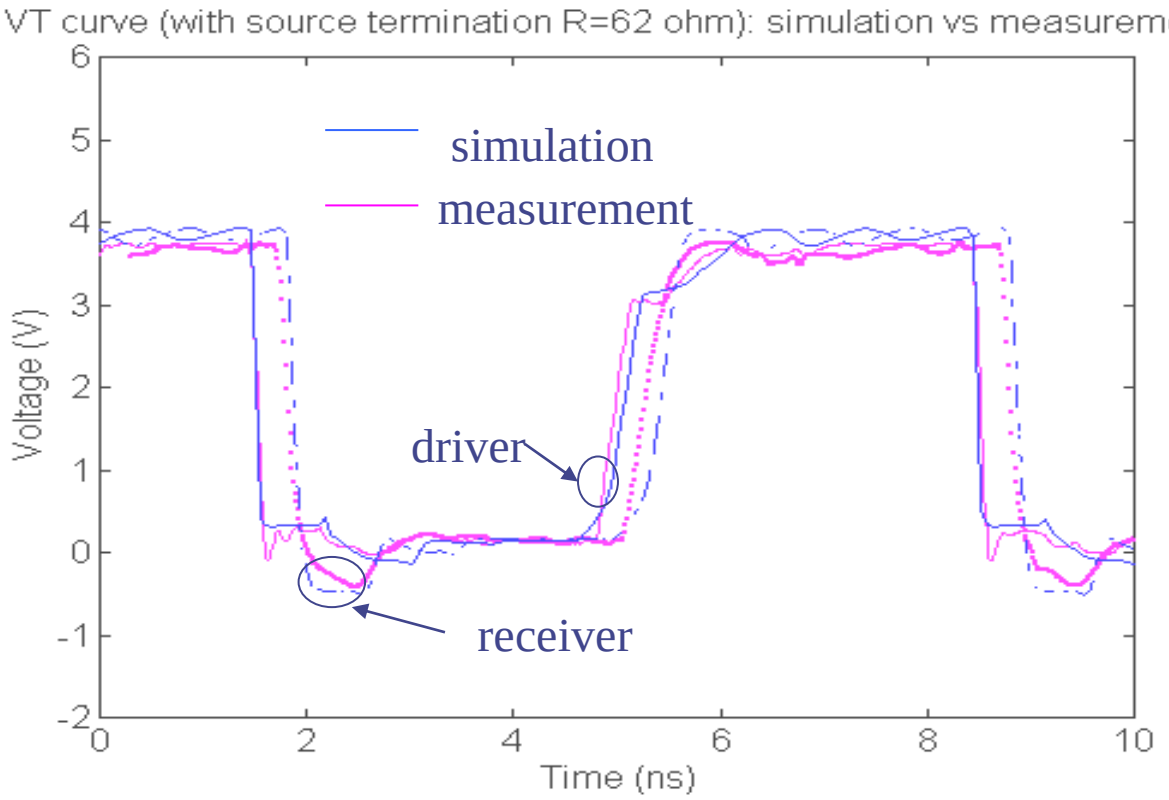
  - Measuring the driver (A) / receiver(B) output with digital oscilloscope (BW=500MHz)

Why do we learn transient response ? (Example: I)

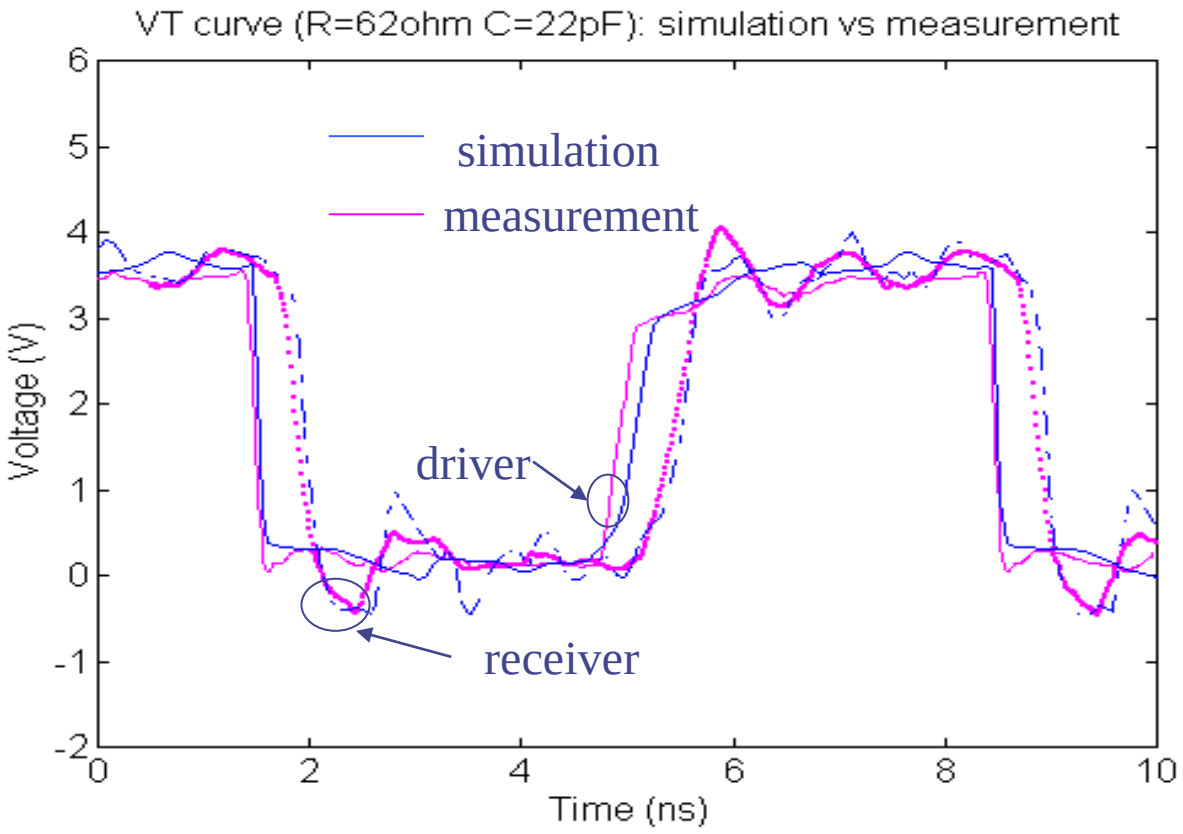
Ringing effect



Why do we learn transient response ? (Example: I)



Why do we learn transient response ? (Example: I)



Why do we learn transient response ? (Rule of Thumb)

Rule of Thumb:

Transmission Line effect should be considered when

$$\text{Length (of transmission)} > \frac{1}{6} \times \frac{T_{rise}}{T_0}$$

For example:

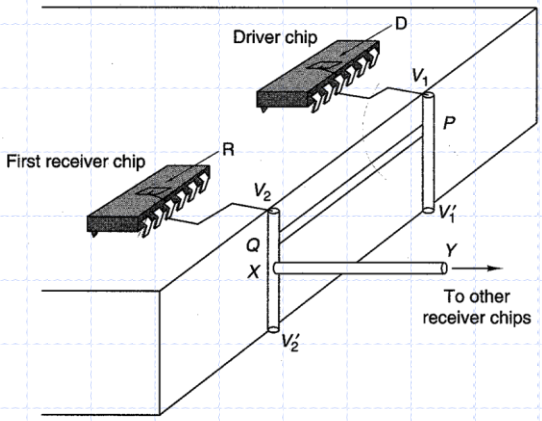
Rambus 28Ω signal line, $T_0 \approx 170\ \text{ps/inch}$

For 200 ps rising edge, $\text{Length} \approx 0.49\text{cm}$!!

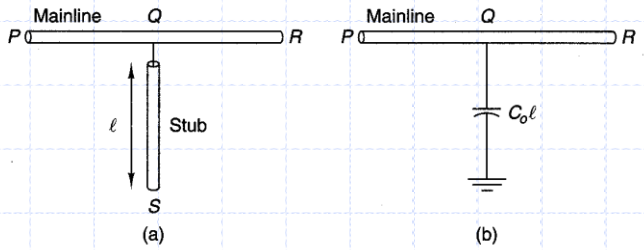
The reflection effect will occur when the Rambus signal Length is longer than 5mm.

Why do we learn transient response ? (Example: II)

- Discontinuity of signal trace (such as stub, via, ..)



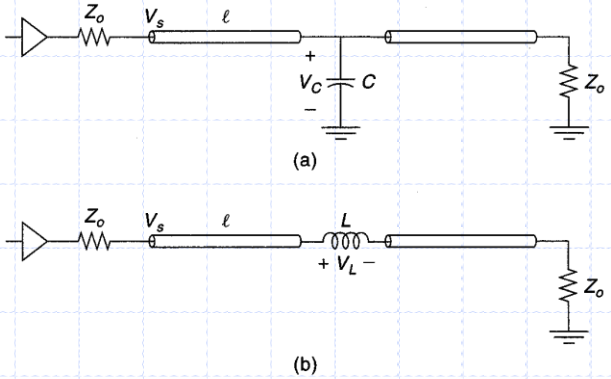
DV_1, RV_2 are metallizations on the board surface. PQ, XY are board internal traces. V_1V_1', V_2V_2' are through vias. The path DV_1PQXY is the mainline, while RV_2Q, PV_1' and XV_2' are stubs.



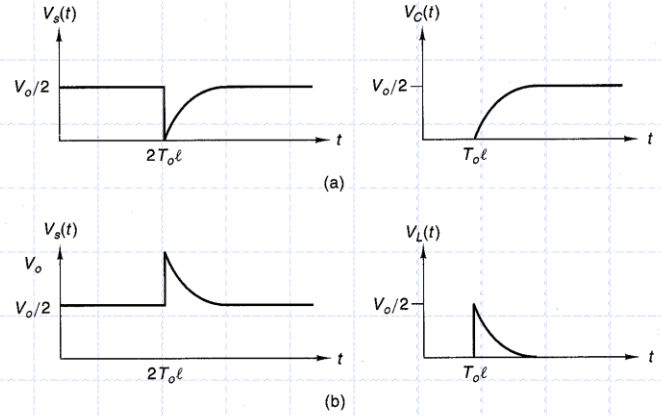
A short stub (a) reflects as a capacitor (b).

Why do we learn transient response ? (Example: II)

- Discontinuity of signal trace (such as stub, via, ..)



Circuit to show reflection from (a) a capacitive and (b) an inductive load.



Waveforms at the source and across the lumped load for (a) a capacitive and (b) an inductor.

Signal Spectra of Square Wave

Periodic square wave pulse train

$$x(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi n \frac{t}{T}) + \sum_{n=1}^{\infty} b_n \sin(2\pi n \frac{t}{T})$$

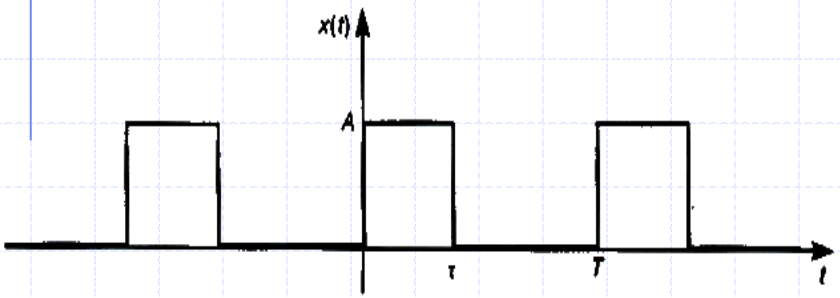


FIGURE 7.4 A periodic "square-wave" pulse train.

$$a_0 = \frac{A\tau}{T}$$

DC term

$$a_n = \frac{A}{n\pi} \sin(2\pi n \frac{\tau}{T})$$

$$b_n = \frac{A}{n\pi}[1 - \cos(2\pi n \frac{\tau}{T})]$$

Amplitude: A
Pulse width: τ
Pulse period: T

Signal Spectra of Square Wave

50% Duty Cycle

Only odd harmonics

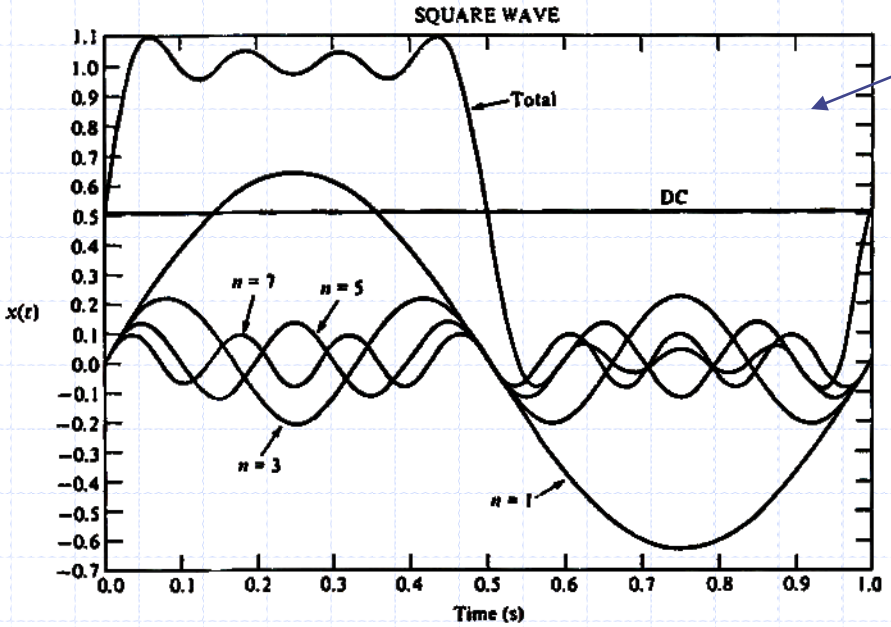
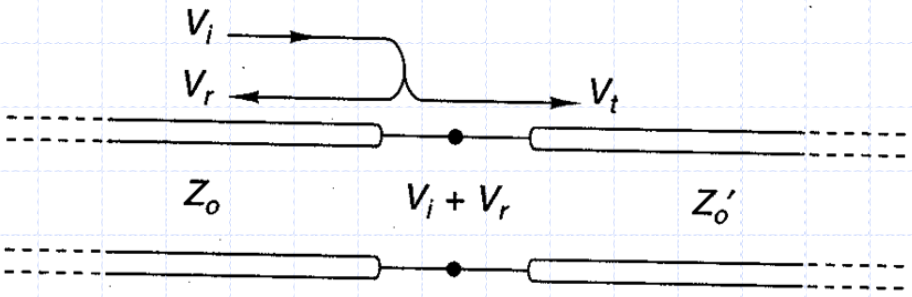


FIGURE 7.5 Illustration of the decomposition of a square wave into its frequency components [1].

Reflection at Discontinuity (impedance discontinuity)

Reflection Coefficient



$$\eta = \frac{V_r}{V_i} = \frac{Z_0^{'} - Z_0}{Z_0^{'} + Z_0} = \text{ Reflection coefficient}$$

$$\mathrm{V_t} = V_i + V_r = (1+\eta)V_i$$

Reflection at Discontinuity (open discontinuity)

$$\eta = \frac{Z_0^{'} - Z_0}{Z_0^{'} - Z_0} = 1$$

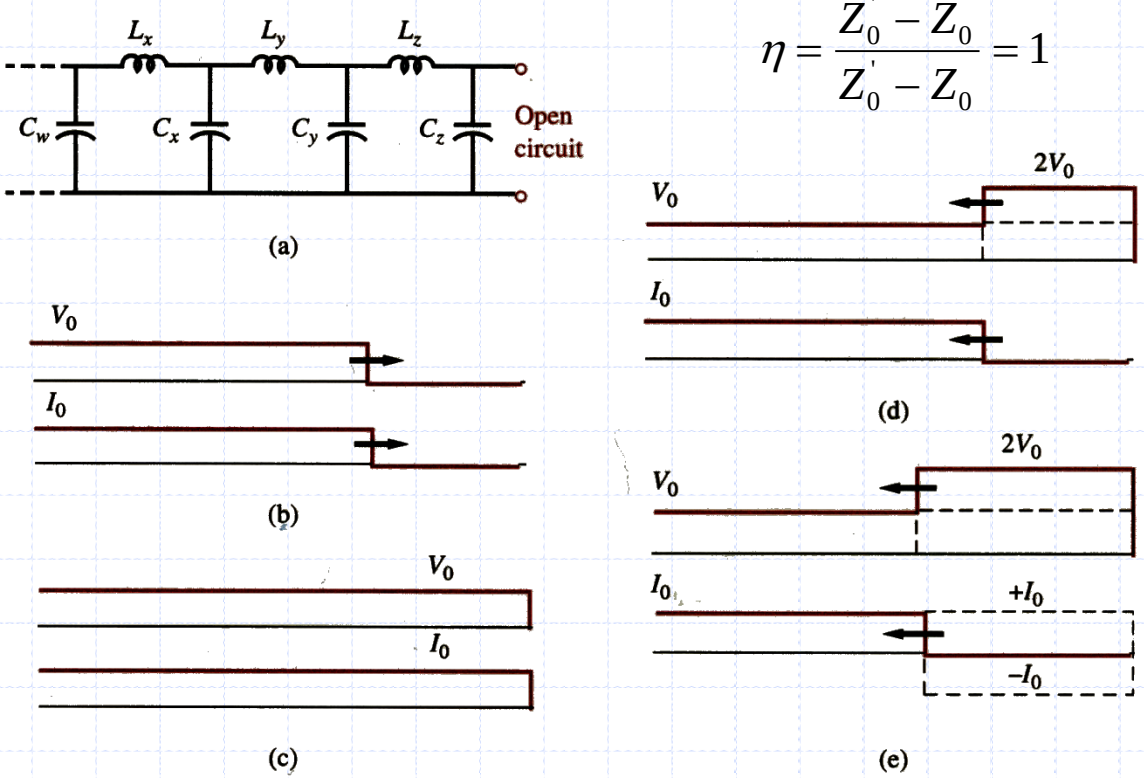
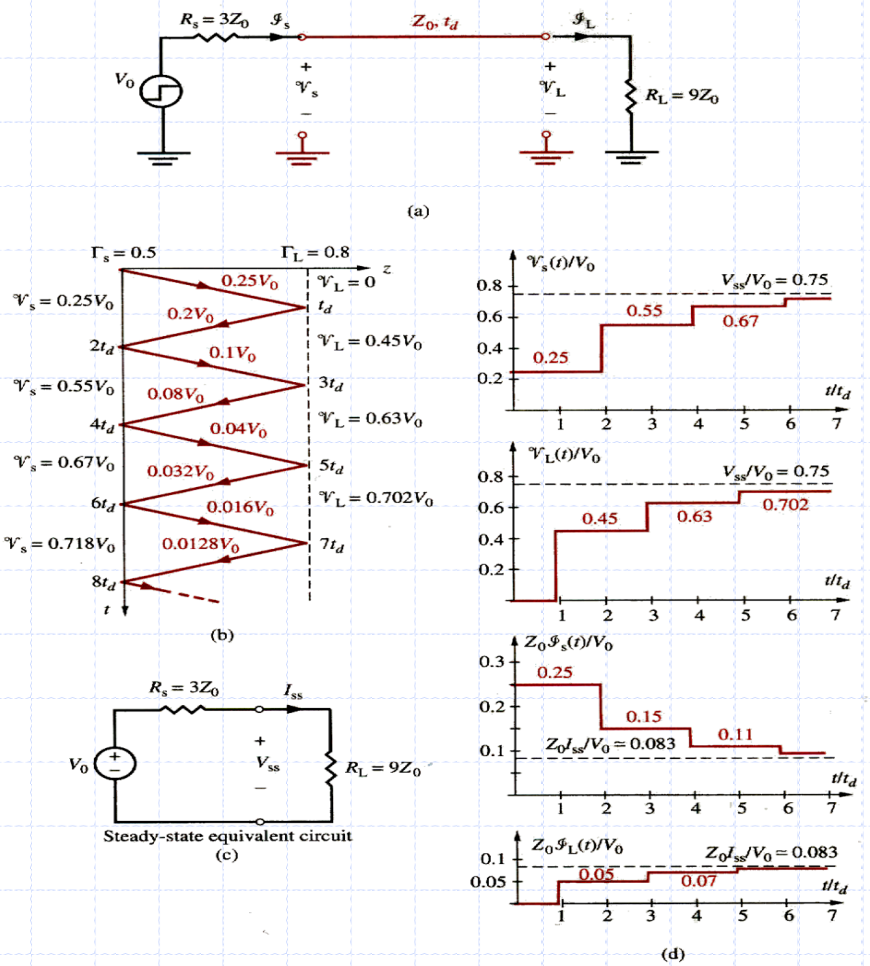


FIGURE 2.10. **The reflection process.** The orderly progress of the disturbances of current and voltage, propagating initially from left to right, is interrupted when they reach the open end of the line, leading to the reflection of the disturbance.

Reflection at Discontinuity (resistive discontinuity)

Bounce diagram



Voltage Transient response at the source end

Voltage Transient response at the load end

Current Transient response at the source end

Current Transient response at the load end

FIGURE 2.17. **Step excitation of a resistively terminated lossless line.** (a) The circuit configuration. (b) Bounce diagram. (c) Steady-state equivalent circuit seen by the source. (d) Normalized source- and load-end voltages and source- and load-end currents as a function of t/t_d.

Reflection at Discontinuity (reactive discontinuity)

- Concept

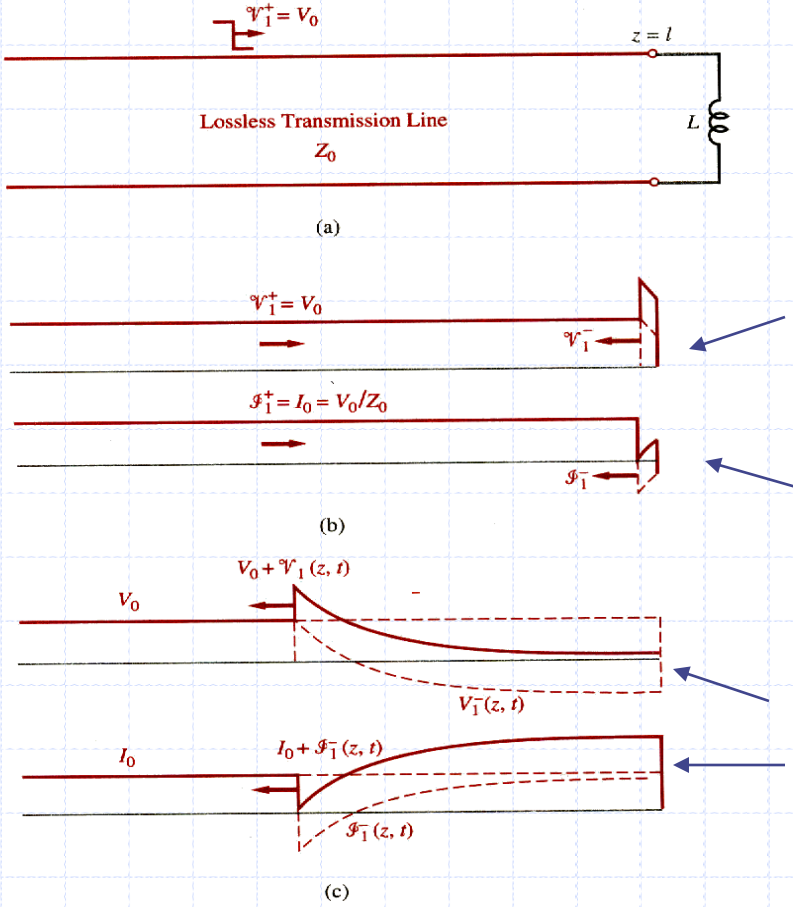


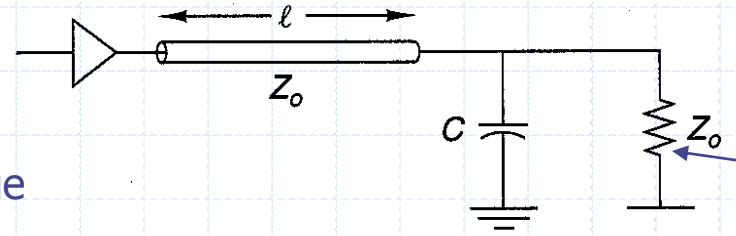
FIGURE 2.24. **Reflection from a purely inductive load.** The source is assumed to be matched (i.e., no reflections back from the source) and to supply a constant voltage V_0. The distributions of the voltage and current are shown at two different times: (b) immediately after reflection when the inductor behaves like an open circuit, and (c) later in time when the inductor behaves as a short circuit.

- Transient step response of an inductor

Reflection coefficient is depend on frequency

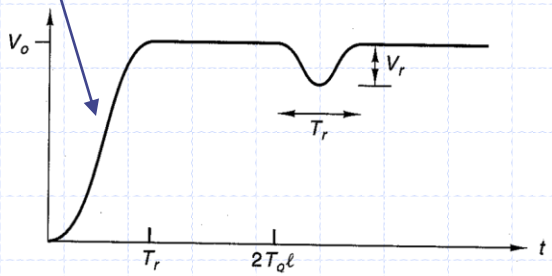
When steady state (DC), inductance acts like a short.

Reflection at Discontinuity (capacitive reactive discontinuity)



Equivalent circuit for Z_0 transmission line

Rising edge



Reflection waveform
by a small shunt capacitance

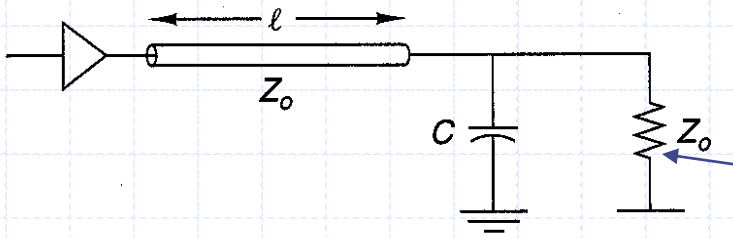
The maximum reflected noise
by the capacitance

$$V_r = -\frac{CZ_0}{2T_r}V_0$$

T_r: Rise time of the input step signal

Reflection at Discontinuity (capacitive reactive discontinuity)

- **Theory**



Equivalent circuit for Z_0 transmission line

$$\eta = \frac{V_r}{V_0} = \frac{Z_L - Z_0}{Z_L - Z_0}$$

$$Z_L = (j\omega C // Z_0) = \frac{Z_0}{1 + j\omega C Z_0}$$

$$\therefore V_r = -\frac{j\omega C Z_0}{2 + j\omega C Z_0} V_0$$

Assume $\left|j\omega C Z_0\right| \le 2$

$$\therefore V_r \approx -\frac{C Z_0}{2}(j\omega V_0)$$

In time domain,

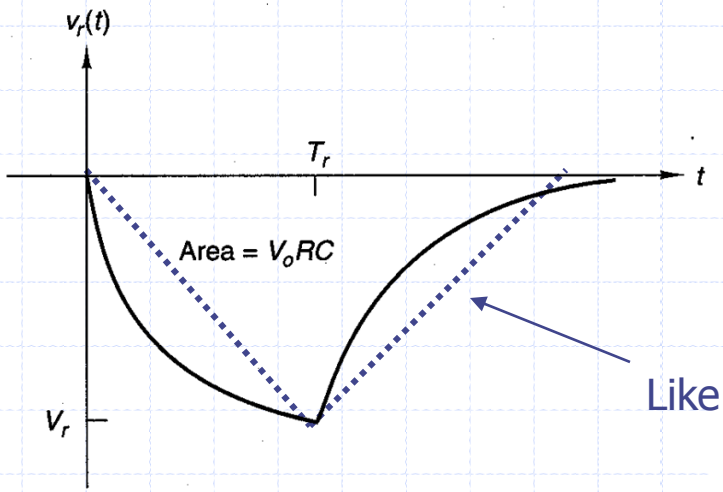
$$v_r(t) \approx -\frac{C Z_0}{2}\left(\frac{d}{dt} v_0(t)\right)$$

$$\therefore \text{The maximum noise } V_r = -\frac{C Z_0}{2 T_r} V_0$$

at the rising edge

Reflection at Discontinuity (capacitive reactive discontinuity)

- **Theory**



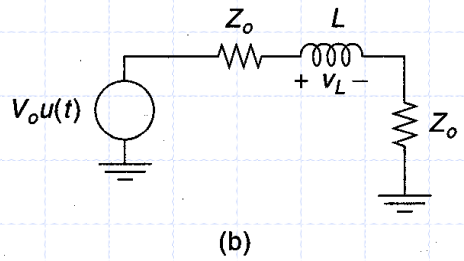
Like a triangular area

It can be proved that the total area under the curve is

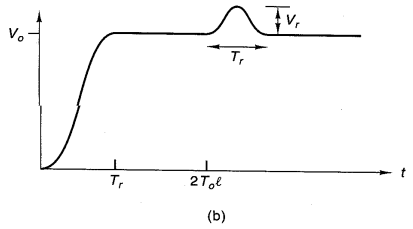
$$\text{area} = \frac{CZ_0}{2T_r}V_0 \times 2T_r \times \frac{1}{2} = C\frac{Z_0}{2}V_0$$

It is independent on the rise time !!

Reflection at Discontinuity (inductive reactive discontinuity)



Equivalent circuit for Z_0 transmission line



Reflection waveform
by a small series inductance

The maximum reflected noise by the inductance

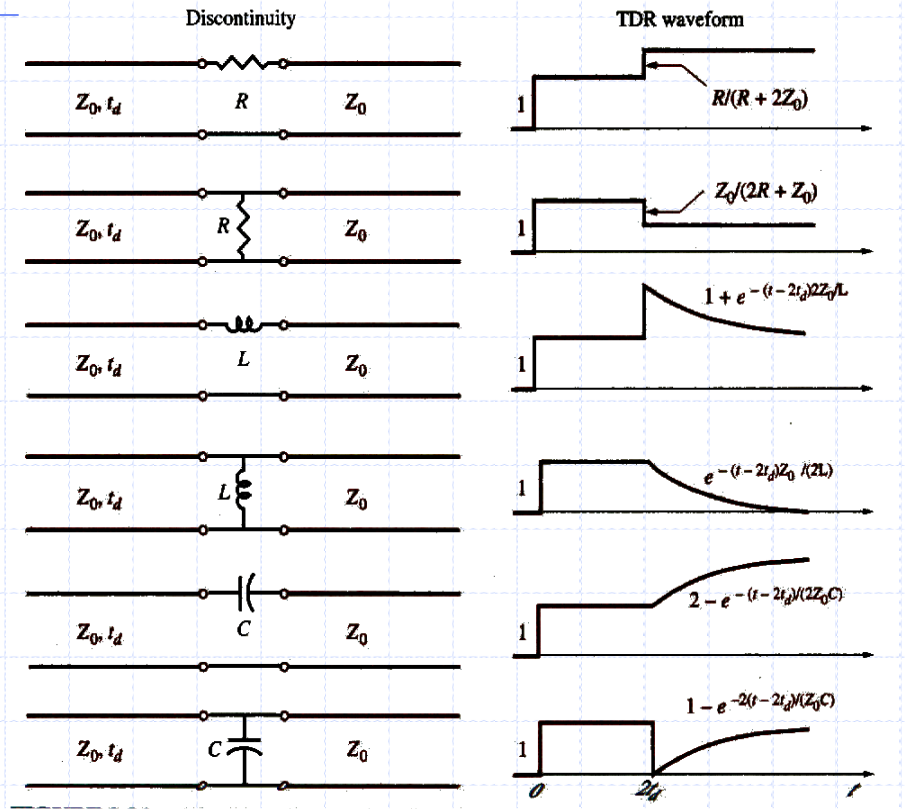
$$V_r = \frac{L}{2Z_0 T_r} V_0$$

T_r: Rise time of the input step signal

Total Area is

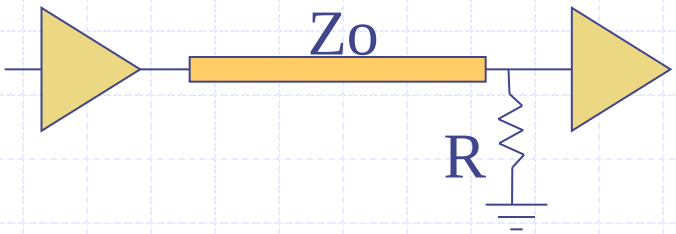
$$A = L\frac{V_0}{2Z_0}$$

TDR signatures produced by simple discontinuities

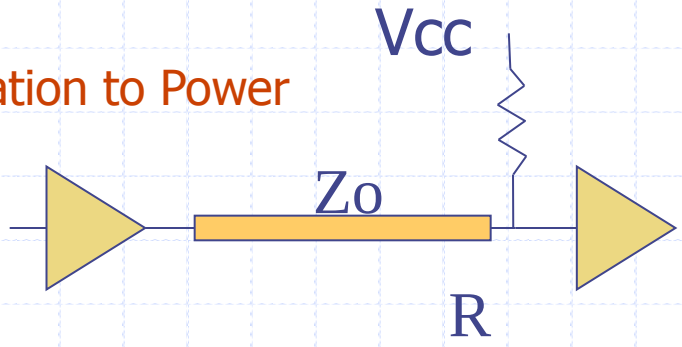


Termination – Parallel termination

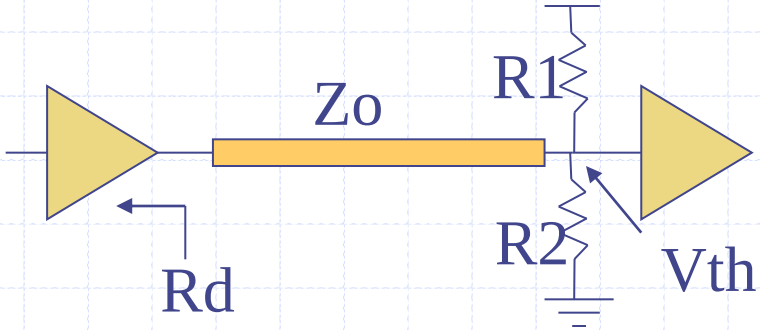
Termination to Ground



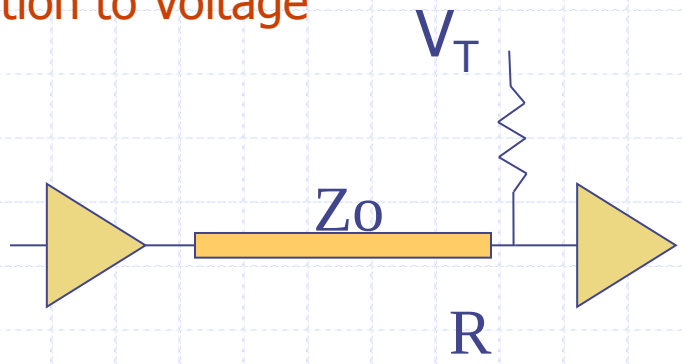
Termination to Power



Thevenin termination

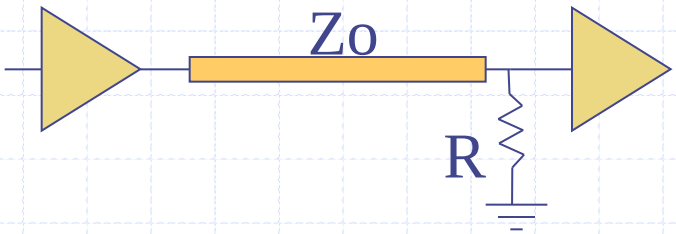


Termination to Voltage



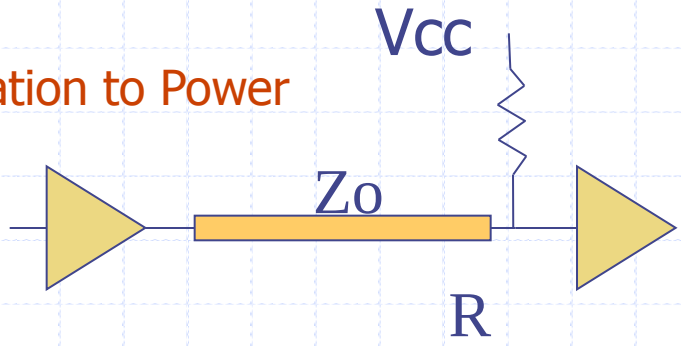
Termination – Parallel termination

Termination to Ground



Design Equation: R=Zo

Termination to Power



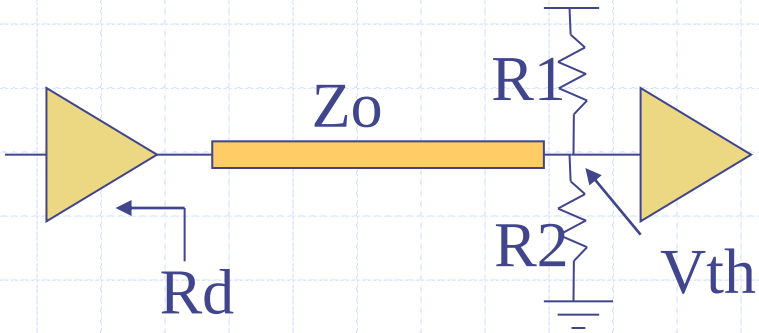
Design Equation: R=Zo

- Advantages:
  - Simplest
- Disadvantage
  - Power consumption
  - Cost R elements and PCB space

Which one is better if you have to choose one ?

Termination – Parallel termination

Thevenin termination



- Advantages:
  - Balanced
- Disadvantage
  - Static Power consumption
  - Cost R elements and PCB space

Design Equations:

Keep I_{oh} and I_{ol} within spec

$V_{th}=V_{oh}(min)-I_{oh}(max)(R_d+Z_o)$

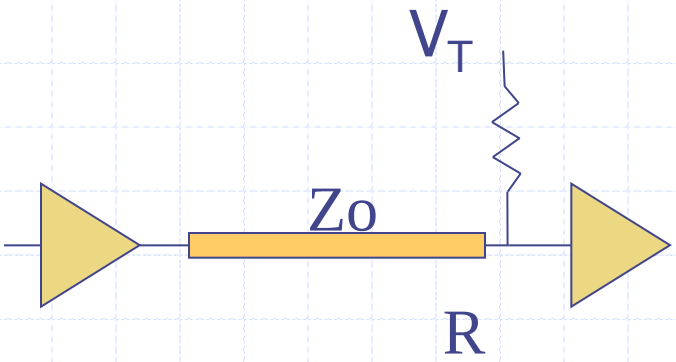
$R_1 // R_2=Z_o$

$R_1=Z_oV_{cc}/V_{th}$

$R_2=Z_oV_{cc}/(V_{cc}-V_{th})$

Termination – Parallel termination

Termination to Voltage

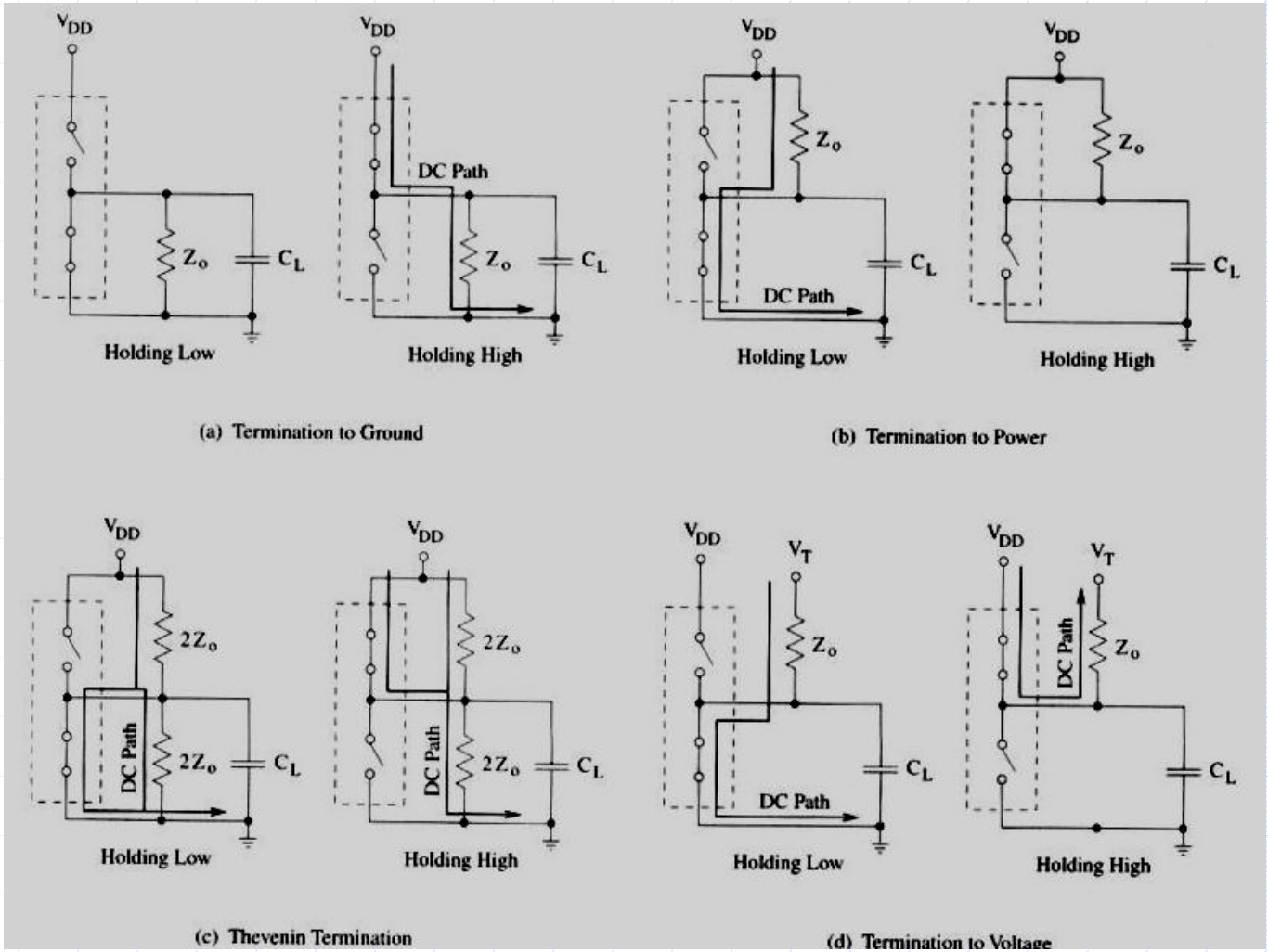


Design Equation: $R=Z_o$

- Advantages:
  - Less static power consumption
- Disadvantage
  - Static Power consumption
  - Cost R elements and PCB space

Termination – Parallel termination

DC current path for totem pole driver



Termination – Parallel termination

Power consumption and DC current

Type	Power	Normalized	Current	Norma
To Power or Ground	$\frac{V_{DD}^2}{R+Z_o}$	1	$\frac{V_{DD}}{R+Z_o}$	1
Thevenin	$\frac{V_{DD}^2(R+2Z_o)}{4Z_o(R+Z_o)}$	$\frac{R+2Z_o}{4Z_o}$	$\frac{V_{DD}}{2(R+Z_o)}$	$\frac{1}{2}$
To Voltage $V_T = \frac{V_{DD}}{2}$	$\frac{V_{DD}^2}{4(R+Z_o)}$	$\frac{1}{4}$	$\frac{V_{DD}}{2(R+Z_o)}$	$\frac{1}{2}$

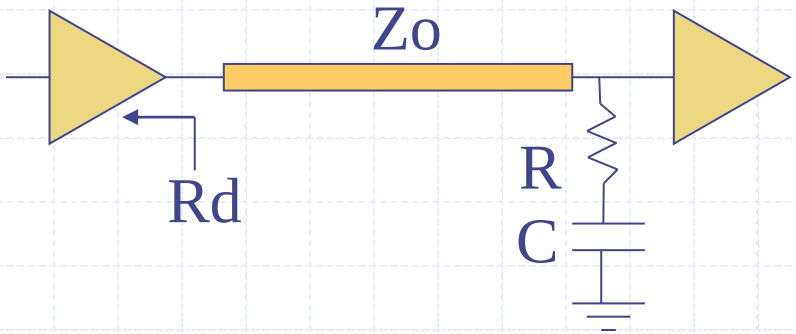
Termination – Parallel termination

Voltage swing

Type	Holding Low	Holding High
Single to Ground	0	$V_{DD}(1-\frac{R}{R+Z_o})$
Single to V_{DD}	$V_{DD}(1-\frac{Z_o}{R+Z_o})$	V_{DD}
Thevenin	$\frac{1}{2}V_{DD}(1-\frac{Z_o}{R+Z_o})$	$\frac{1}{2}V_{DD}(1+\frac{Z_o}{R+Z_o})$
To Voltage $V_T=\frac{V_{DD}}{2}$	$\frac{1}{2}V_{DD}(1-\frac{Z_o}{R+Z_o})$	$\frac{1}{2}V_{DD}(1+\frac{Z_o}{R+Z_o})$

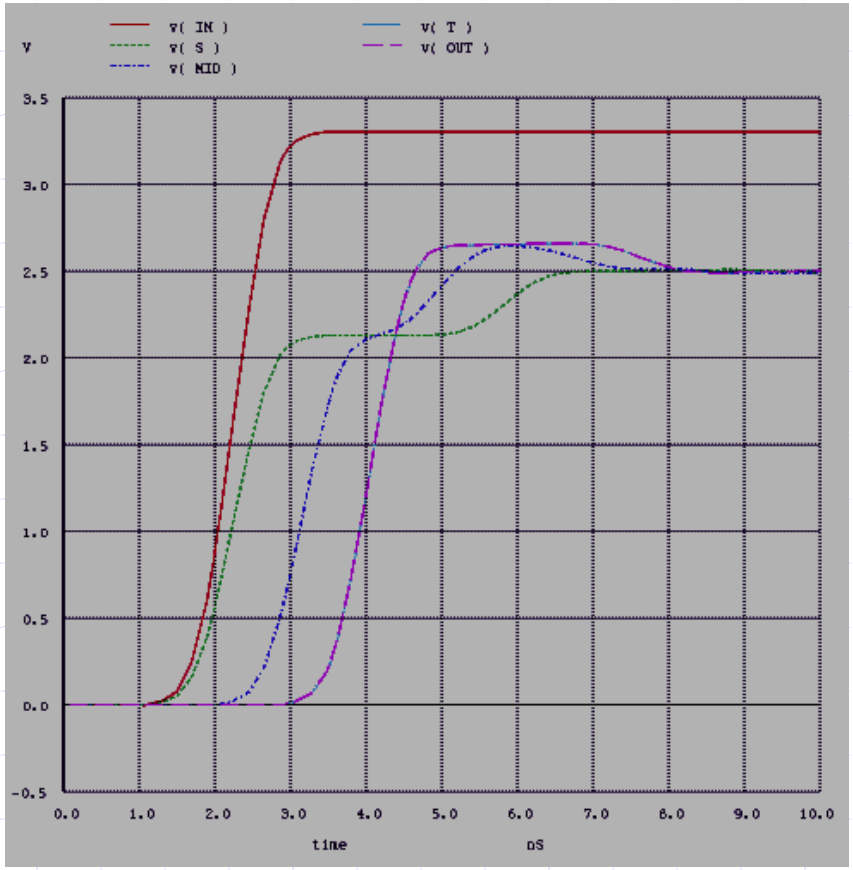
- To obtain the maximum noise margin, the widest noise swing is required
- The maximum swing is got when R << Z0.
- But it will cause a large reflection at source and high power dissipation.

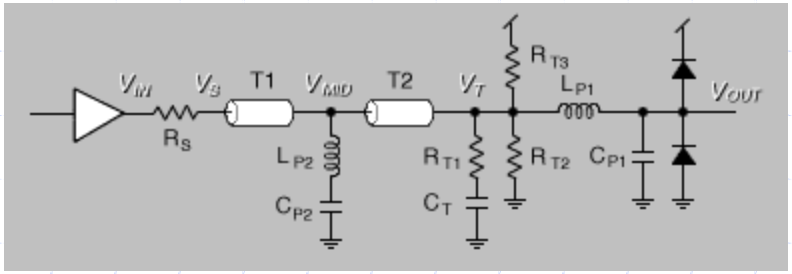
Termination – AC termination



- Advantage:
  - Power saving
- Disadvantage:
  - Data line may exhibit time jitter (depend on previous pattern)
  - C is not easy to design
- Application
  - Battery-driven systems

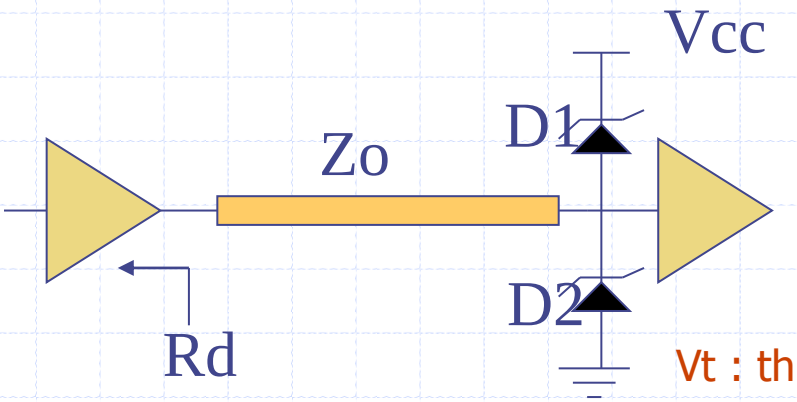
Termination – AC termination





Driver parameters	Driver	Ideal voltage source				
	Rise / fall time	1000	ps	Step amp. 3.3	V	Polarity Rising
Series termination	R_S	37.5	ohms			
Line parameters	T_1 length	15	cm	$Z_{0\,1}$ 68	ohms	$e_{eff\,1}$ 3.2
	T_2 length	15	cm	$Z_{0\,2}$ 68	ohms	$e_{eff\,2}$ 3.2
Line loading	L_{P2}	0	nH	C_{P2} 0	pF	
AC termination	R_{T1}	111	ohms	C_{T1} 1000	pF	
Parallel / Thevenin termination	R_{T2}	1000K	ohms	R_{T3} 1000K	ohms	
Clamp diode termination	Clamp	Neither		V_{CC} 3.3	V	
Receiver parasitics	L_{P1}	0	nH	C_{P1} 0	pF	

Termination – diode termination

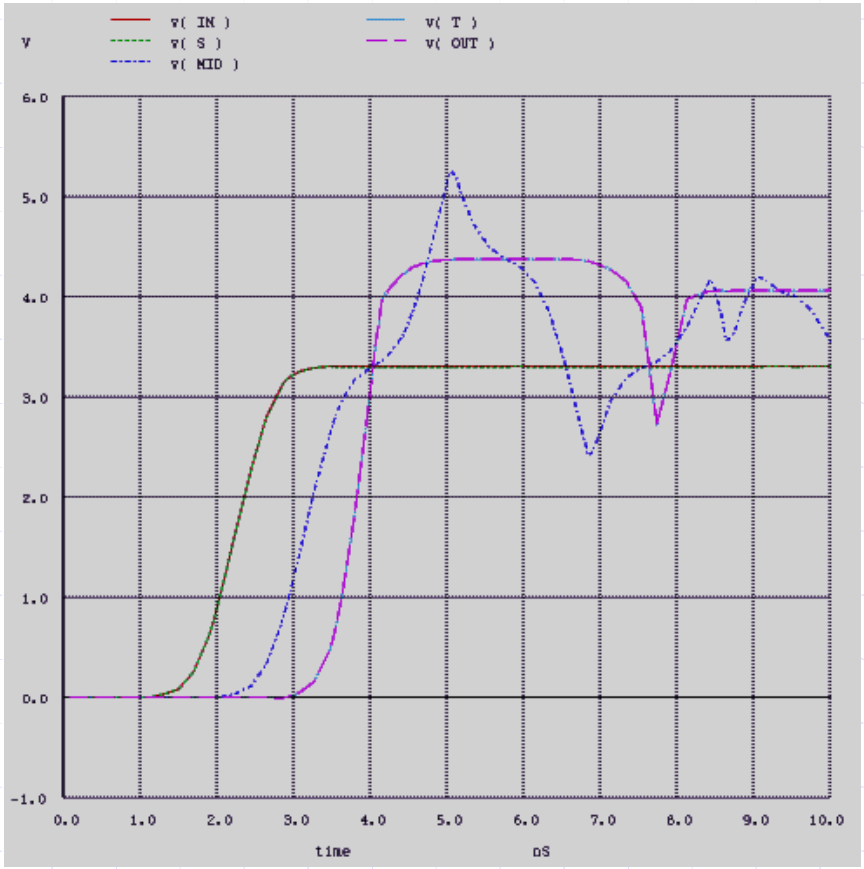


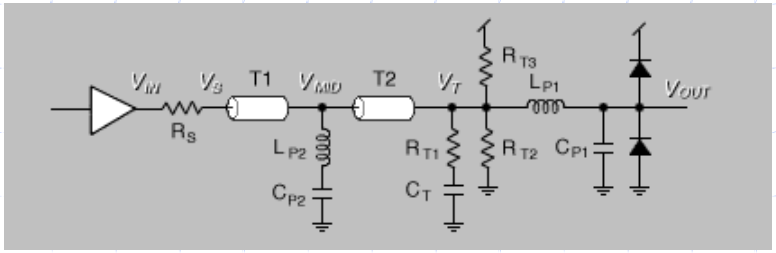
The V(out) is limited to Vcc+Vt to -Vt

Vt : threshold voltage of the diode

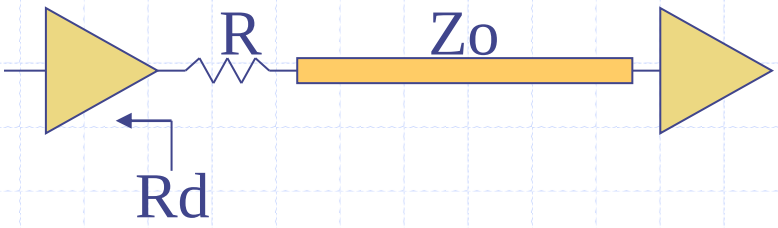
- Advantage:
  - Require no matching (large impedance variation)
  - Lower power dissipation
  - Standard ESD protection circuit include diode clamping in the configuration identical the diode termination
- Disadvantage
  - Existence of multiple reflection

Termination – diode termination



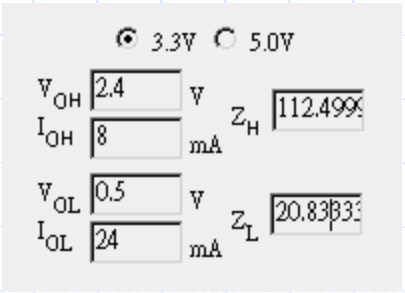


Termination – series termination

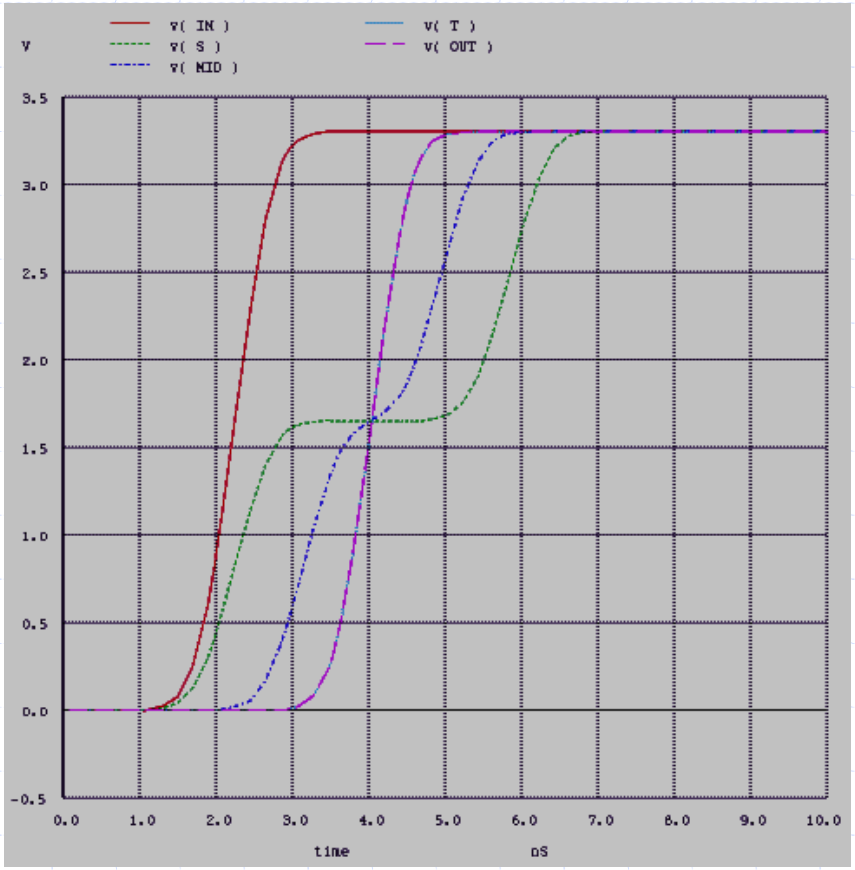


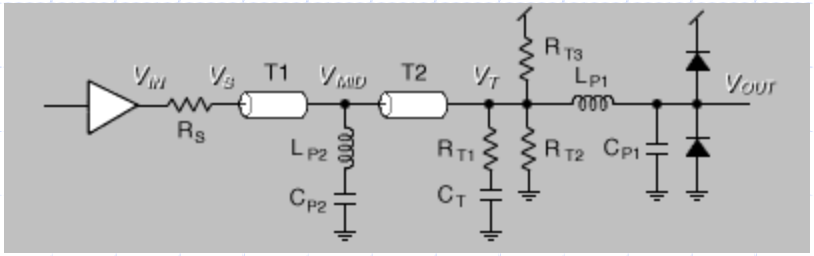
Design Equation: $R=Z_o-R_d$

- Advantages:
  - Simple
  - Consume less power
- Disadvantage
  - The R_d is different for Pull-up and Pull-down
  - Reduce noise immunity in a multi-drop bus situation (such as clock chain)
  - Because of half voltage is launched into the transmission line)



Termination – series termination



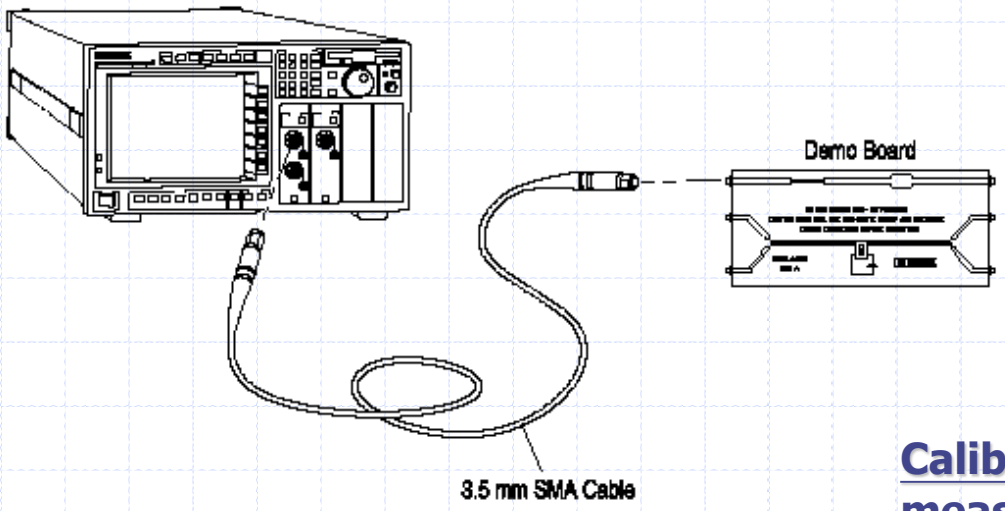


Termination

In practical design, which one is better ?

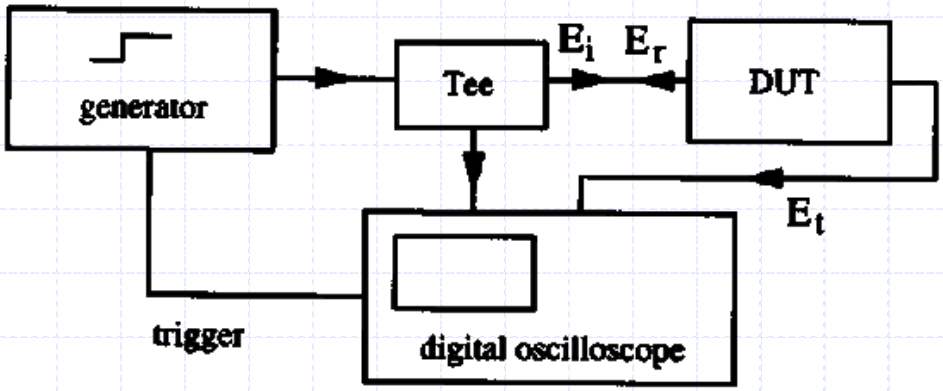
1. None
2. Series
3. AC
4. parallel

Time Domain Reflectometry



Bandwidth : 20GHz
Min. rising time: 38ps

Calibration of error in TDR measurement is quite important

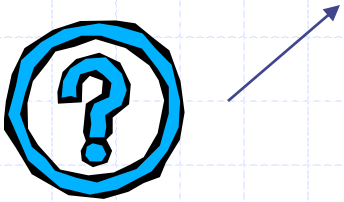


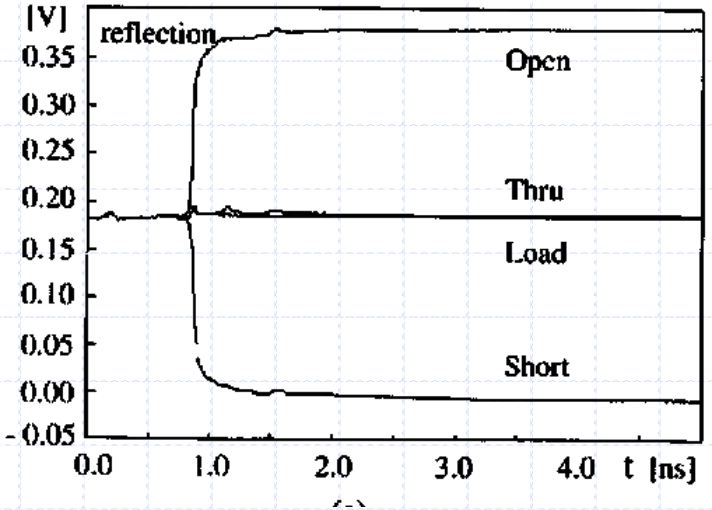
Time Domain Reflectometry (Calibration)

Before accurate impedance measurements can be performed, the frequency response errors and losses caused by the imperfections in the system, cables, and probing hardware must be removed by the **calibration.**

Procedures:

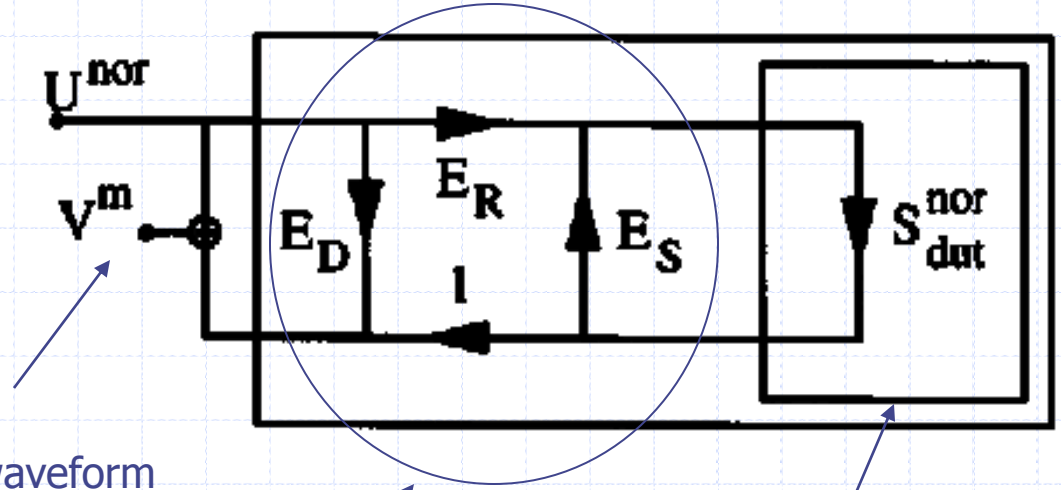
1. Short
2. Load (50 ohm)
3. Open





Time Domain Reflectometry (Calibration)

Principles of calibration



Measured waveform in TDR

Errors (cables, connectors, probes)

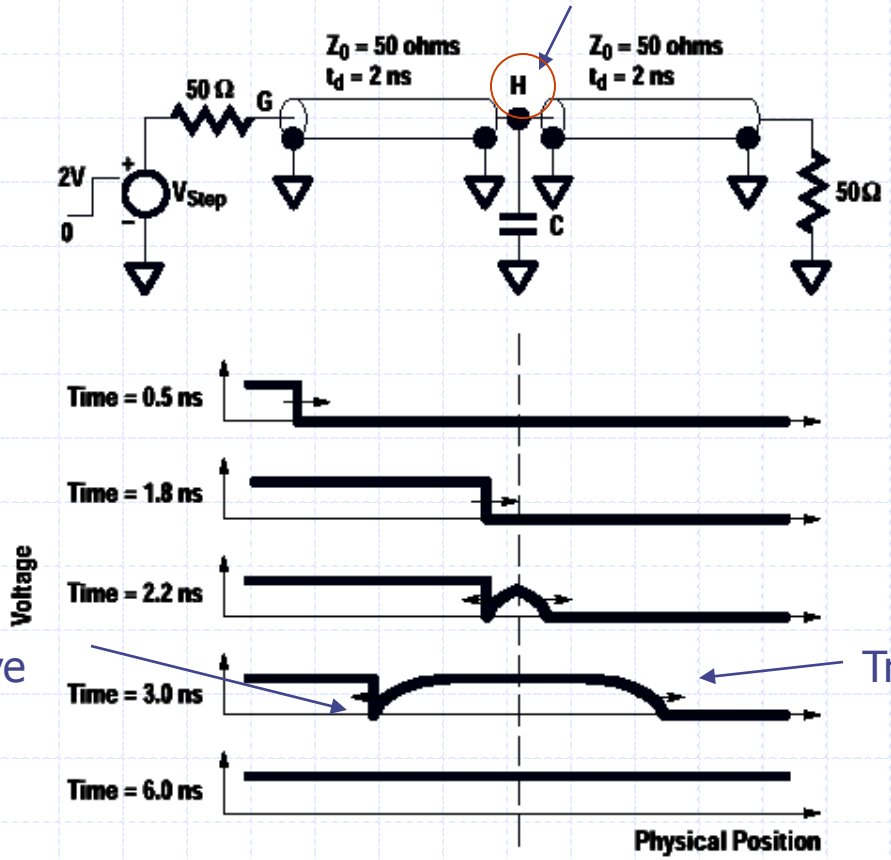
Device under test

TDR measurement (Impedance Profile measurement)

TDR measurement (Parasitic capacitance measurement)

- Discrete shunt capacitance

The voltage distribution v.s. time at point H

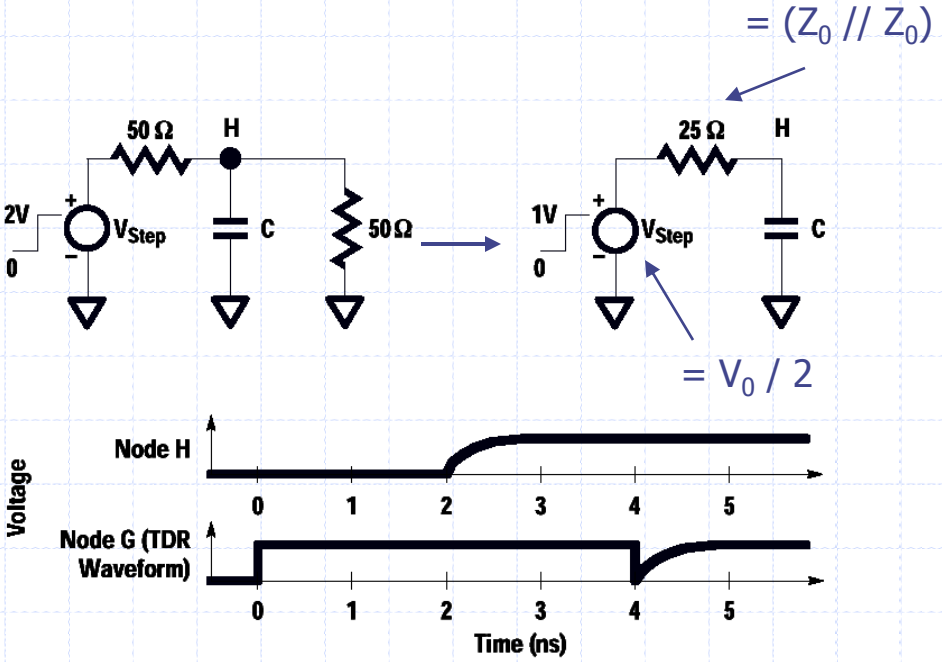


Reflected wave

Transmitted wave

TDR measurement (Parasitic capacitance measurement)

The equivalent circuit at point H



The transmitted wave at point H

$$V_H(t) = \frac{V_0}{2}(1 - e^{-t/\tau})$$

$$\text{where } \tau = RC = \frac{Z_0}{2}C$$

$$V_H(t) = \frac{V_0}{2} + V_{ref}(t)$$

= Incident wave + Reflected wave

= Transmitted wave

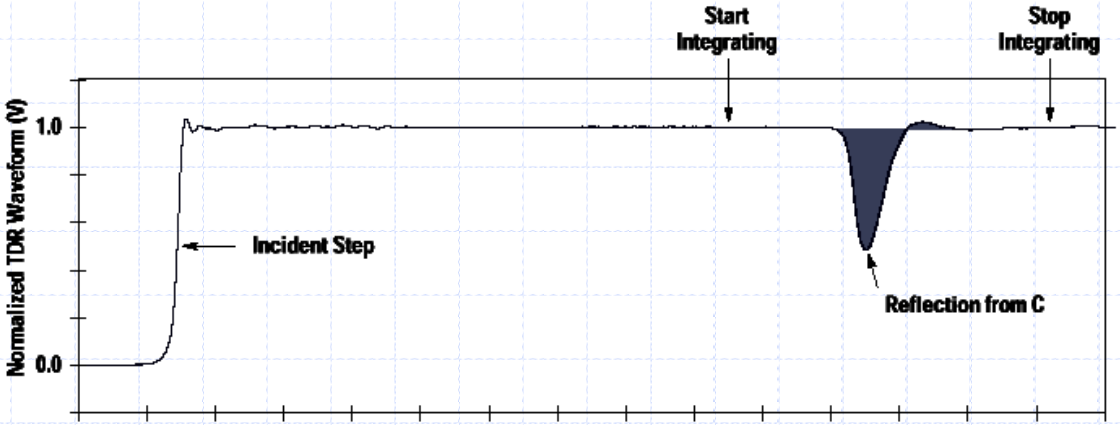
The reflected wave is

$$V_{ref}(t) = -\frac{V_0}{2}e^{-t/\tau}$$

TDR measurement (Parasitic capacitance measurement)

$$A = \int_{\infty}^{\infty} \mathrm{V}_{\mathrm{ref}}(t)dt = \int_{\infty}^{\infty} -\frac{V_0}{2} e^{-t/\tau} dt = -\frac{V_0}{2}\tau = -\frac{V_0}{2}\left(\frac{Z_0}{2}C\right)$$

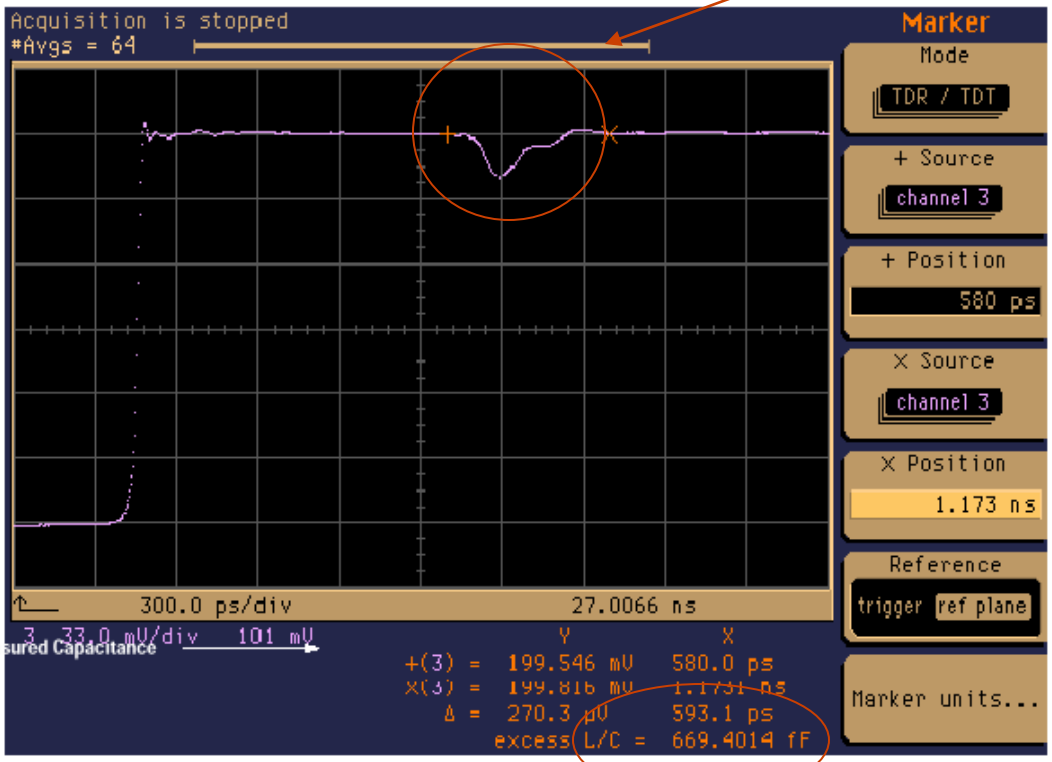
$$\therefore C = -\left(\frac{2}{Z_0} \times A\right) \times \frac{2}{V_0}$$



TDR measurement (Parasitic capacitance measurement)

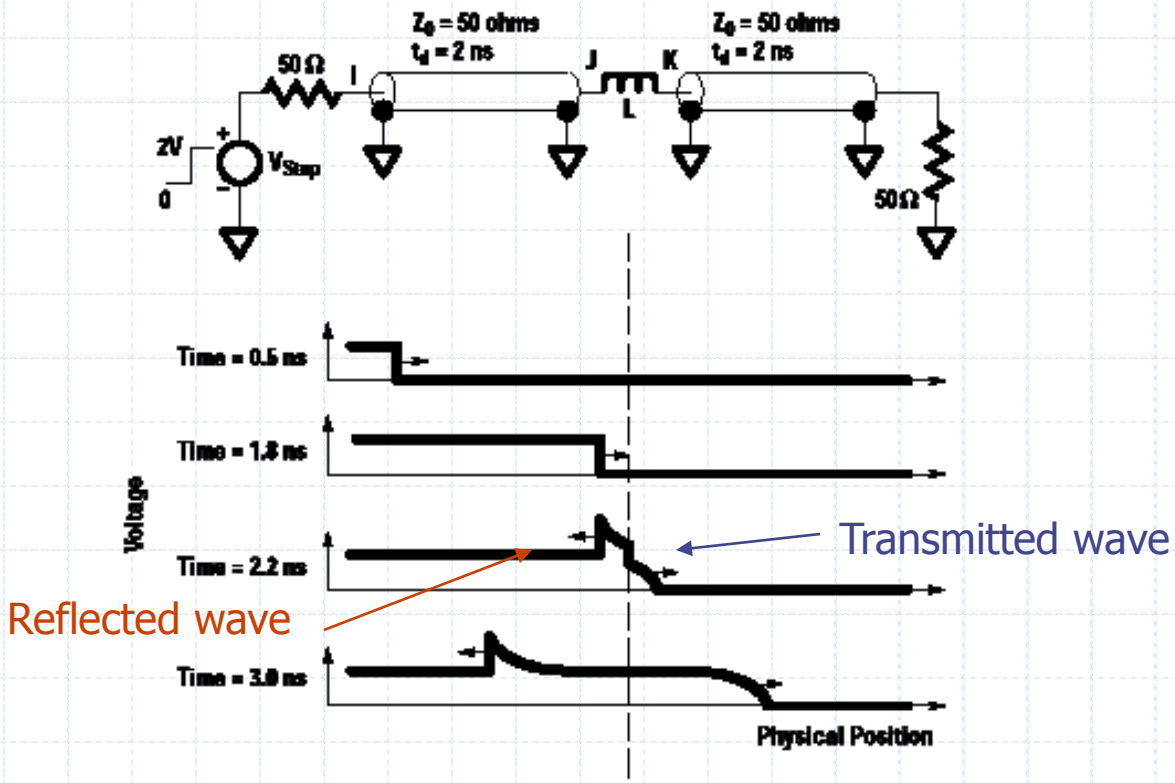
- TDR signature by HP TDR/TDT

Capacitance effect



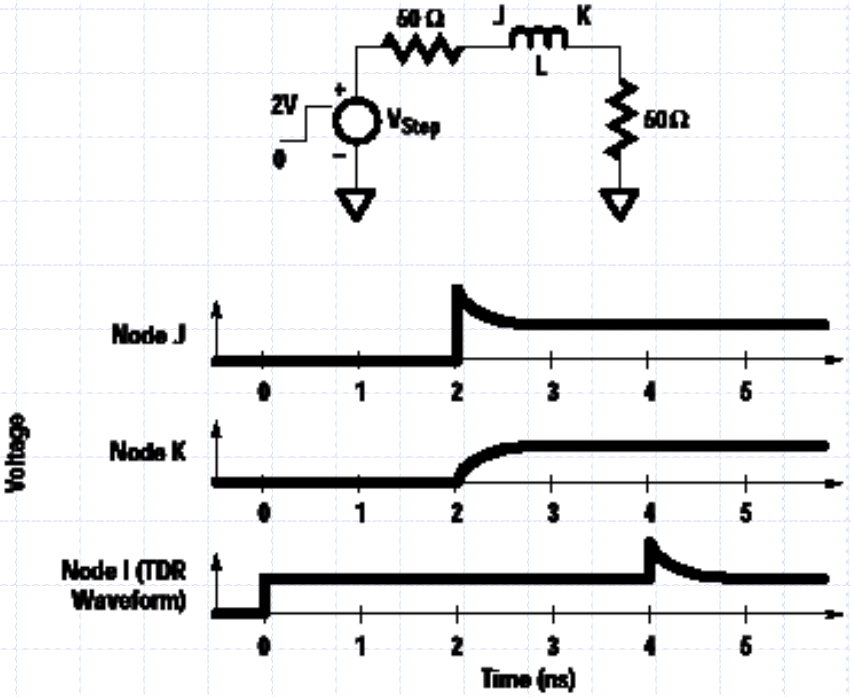
Capacitance value

TDR measurement (Parasitic inductance measurement)



TDR measurement (Parasitic inductance measurement)

- Equivalent circuit seen between J and K



The transmitted wave at point J

$$V_j = \frac{V_0}{2}(1+e^{-t/\tau})$$

$$V_k = \frac{V_0}{2}(1-e^{-t/\tau})$$

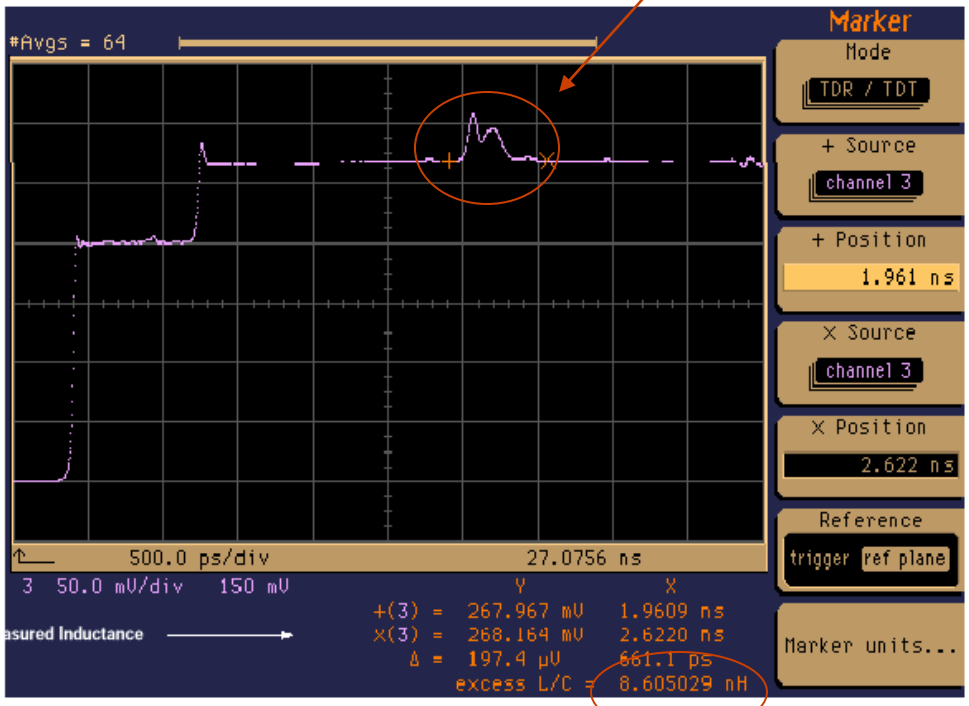
$$\text{where } \tau = \frac{\mathrm{L}}{\mathrm{R}} = \frac{L}{2Z_0}$$

The reflected wave is

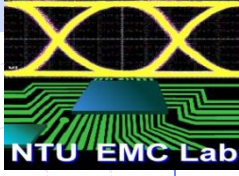
$$\frac{V_0}{2}e^{-t/\tau}$$

TDR measurement (Parasitic inductance measurement)

Inductance signature

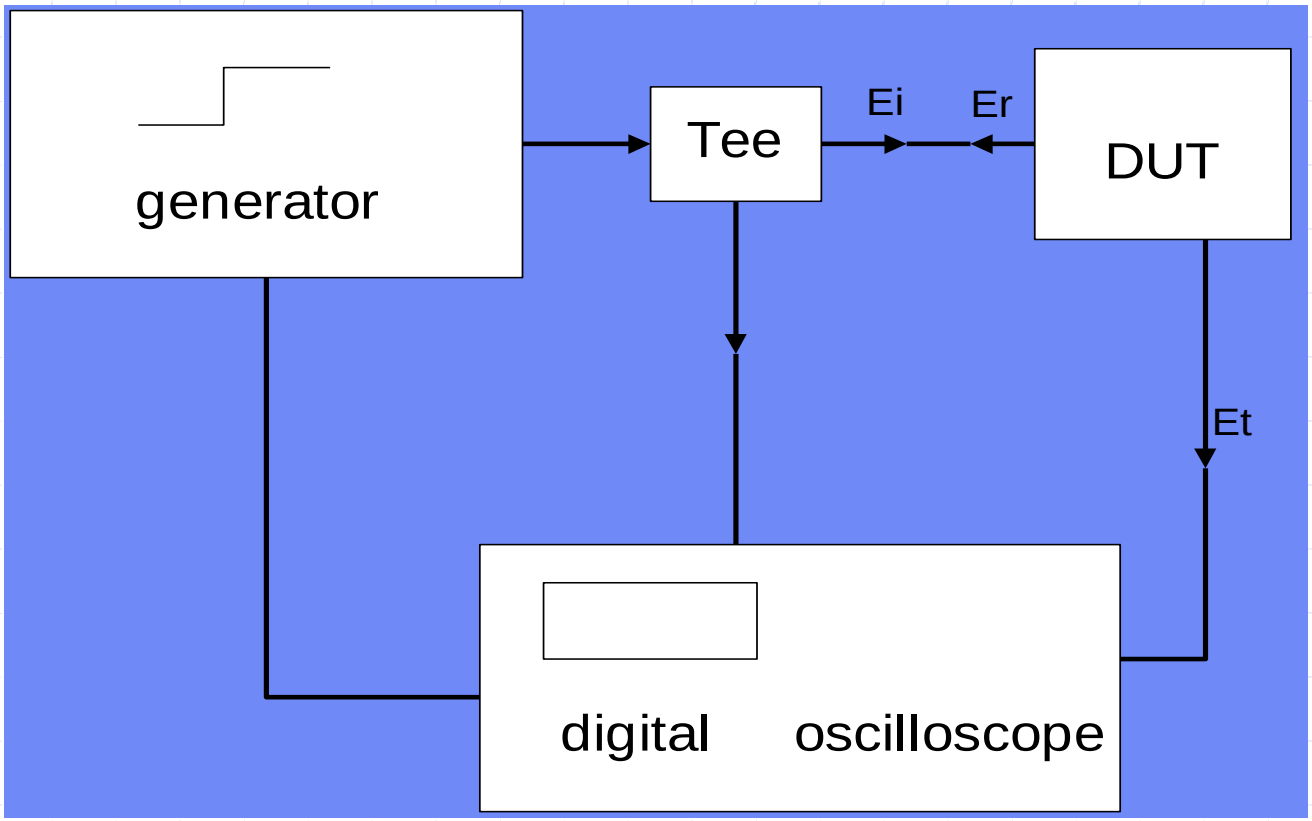


Inductance value



時域網路分析儀的校正

時域網路分析儀之方塊圖



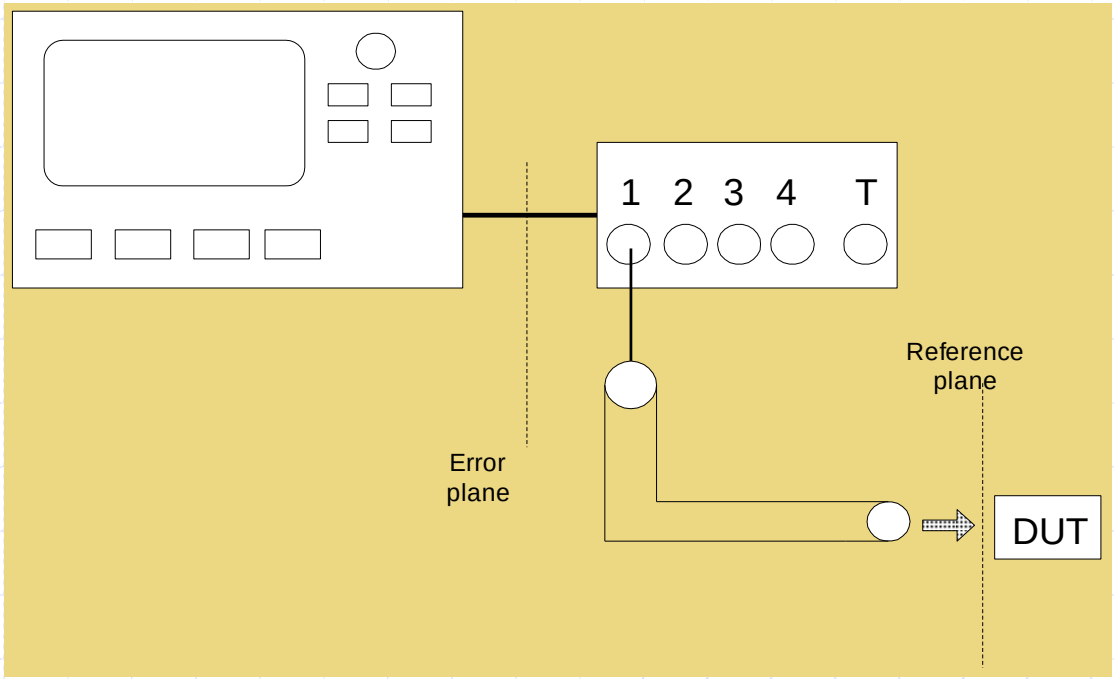
在時域下量測的優點

時域反射波形可輕易察覺出待測物的不連續處，例如訊號中斷或訊號失真處，也可確定出傳輸線之特性阻抗，進一步處理便可萃取出其等效之電容電感值，而且由時域反射量測也可求出待測物的返回損耗（return loss）、駐波比（VSWR，即standing wave ratio）和反射係數。另一方面，時域透射量測被用來求得訊號在待測物的傳遞時間、增益或損耗和穿透係數。

需要校正的原因

在做量測時待測物和時域網路分析儀需用轉接頭（connector）和同軸傳輸線（coaxial cable）相連接，而有不必要的傳播延遲（propagation delay）和損耗現象發生，有時是示波器內部所導致的損耗誤差，如此的現象會使得量測值和實際值會有明顯的差距，所以要把這些不必要的現象修正而得到確實想要的資料，就需要做校正（calibration）的動作。

目前在時域下還沒有精確的校正技術，故在無校正下不同的量測狀況測量同一待測物往往結果並不相同，如此就限制了時域量測的實用性，所以我們在校正技術時採用頻域網路分析下的全雙埠誤差模型（Full two port error model）求出系統的誤差來源並加以移除使之量測結果有如在待測物前的參考平面測得一般，見下圖。



校正平面示意圖

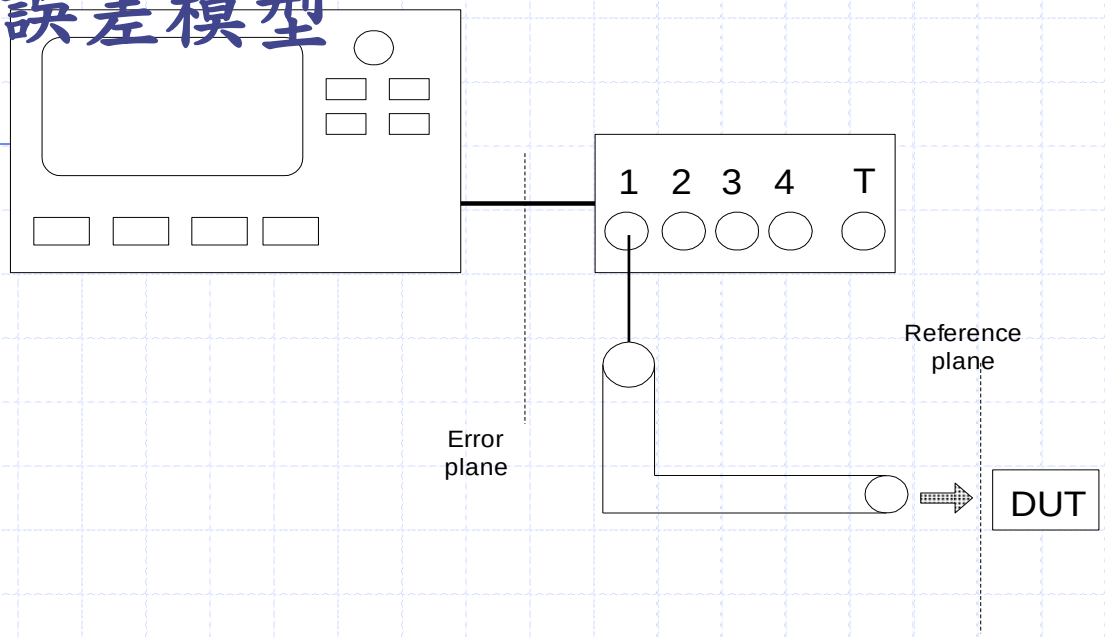
校正步驟分為以下三步驟：

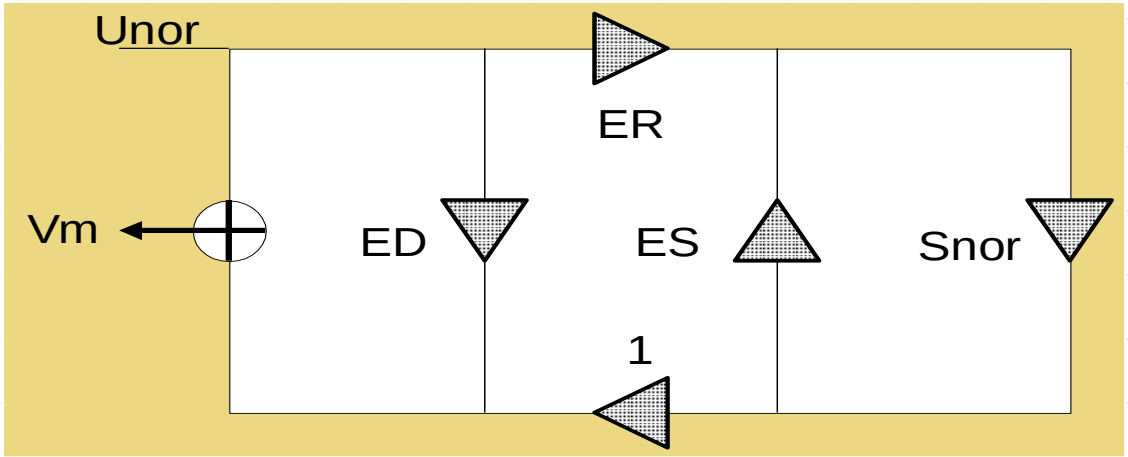
1.由時域量測得我們所需之時域信號，然後轉換至頻域

2.藉由頻域資料來決定誤差網路中的各個參數，接著便可計算出校正後待測物的散射參數，而此時也可把所得資料作正規化處理。

3.將校正後和正規化後得的資料轉換回時域。

單埠網路誤差模型





單埠誤差模型的信號流程圖

ED（the directivity）：指向性誤差

ES（the source impedance match）:信號源不匹配誤差

ER（the reflection frequency response）:反射路徑誤差，也稱做 reflection tracking

$$ES \times (S_{\text{nor}} \times X) + U_{\text{nor}} \times ER = X$$

$$\rightarrow X = U_{\text{nor}} \times ER \div (1 - S_{\text{nor}} \times ES)$$

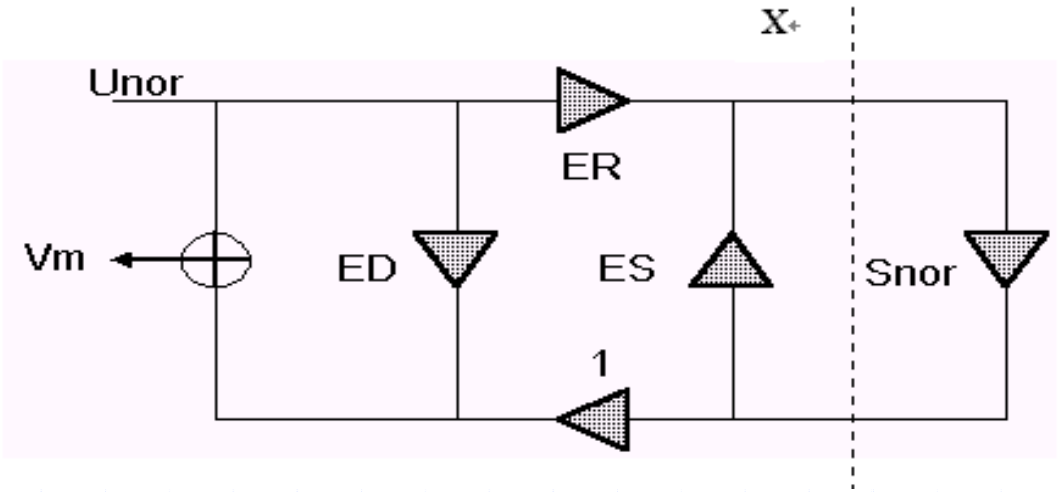
$$\rightarrow V_m = (1 + ED) \times U_{\text{nor}} + X \times S_{\text{nor}}$$

$$V_{\text{m}} = ED' + S_{\text{nor}} \times ER' / (1 - ES \times S_{\text{nor}})$$

$$ED' = (1 + ED) \times U_{nor}$$

$$ER' = ER \times U_{nor}$$

$$V_m = ED' + (ER' - ED' \times ES) \times S_{nor} + ES \times S_{nor} \times V_m$$

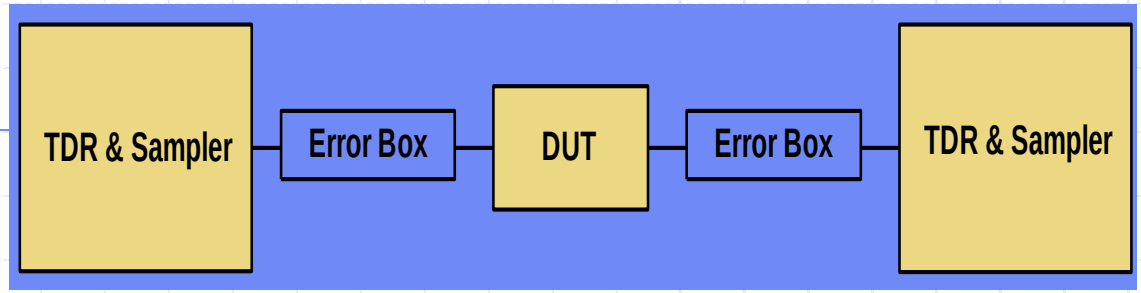


此時我們採用SOLT參考標準（SOLT-reference standards），就是把待測物用短路（short）校正器、開路(open)校正器和50歐姆負載（load）校正器取代後而得的資料，我們分別表示為 $V^m_{short}, V^m_{open}, V^m_{load}$ 但這僅止於單埠校正，若要做雙埠校正便需要把連接待測物的兩端接頭對接（thru）後的資料。

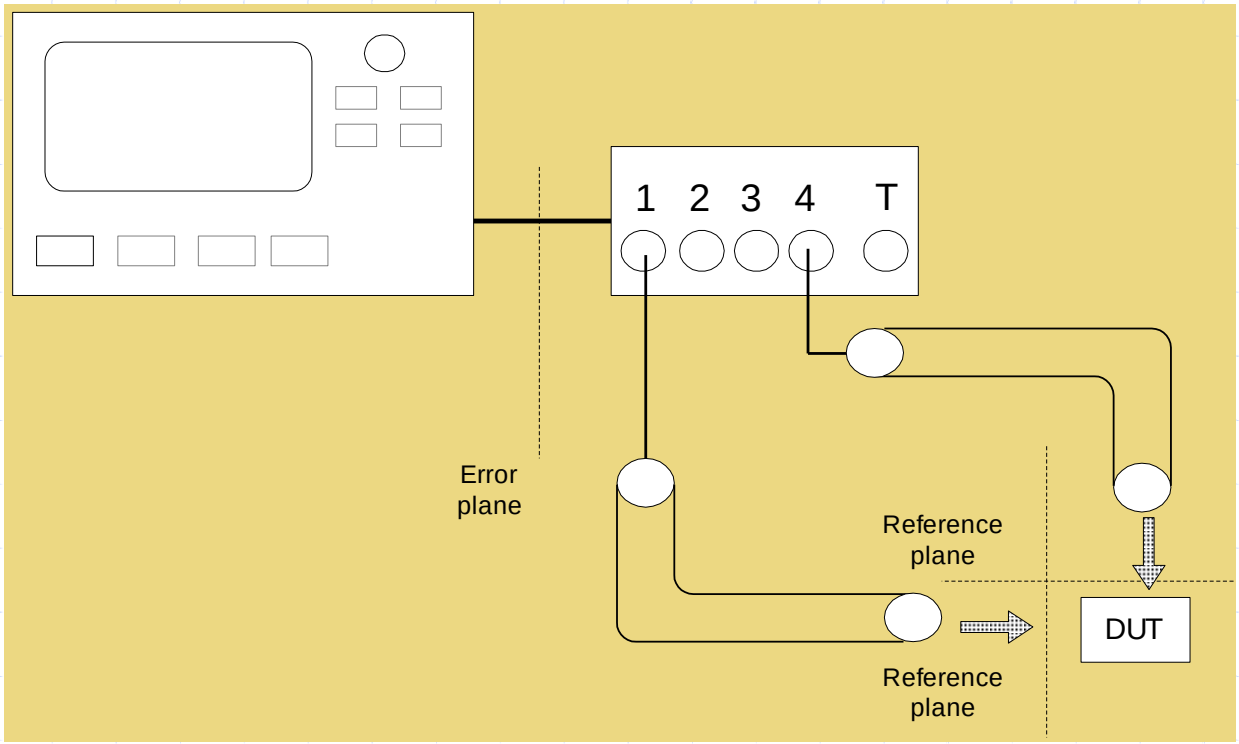
$$S_{\text{dut}} = \frac{(V_m - ED')}{ES(V_m - ED') + ER'}$$

$$V_{nor} = \frac{(V_m - ED') \times U_{nor}}{ES(V_m - ED') + ER'} + U_{nor}$$

雙埠網路誤差模型

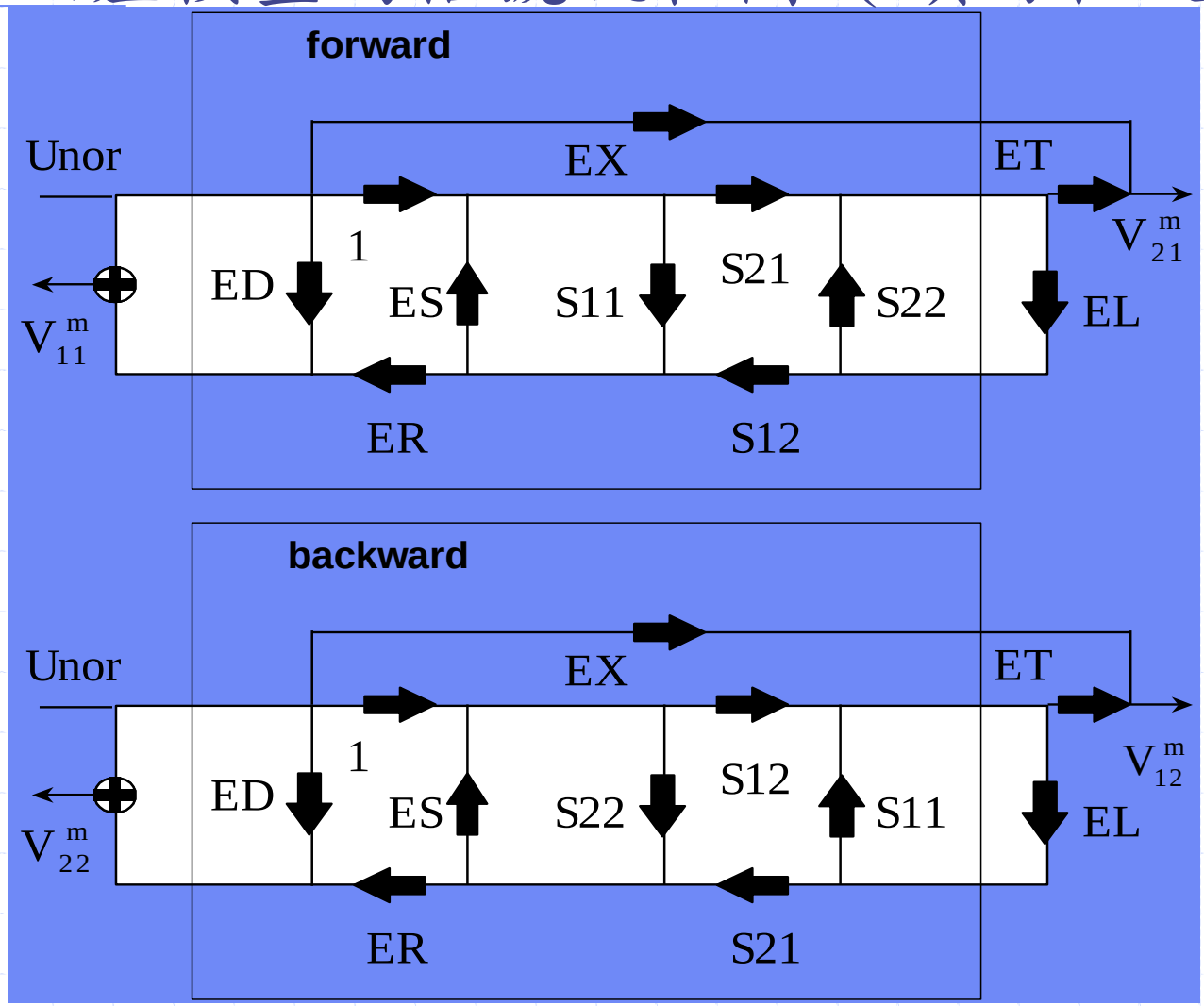


雙埠量測系統之方塊圖



雙埠量測系統

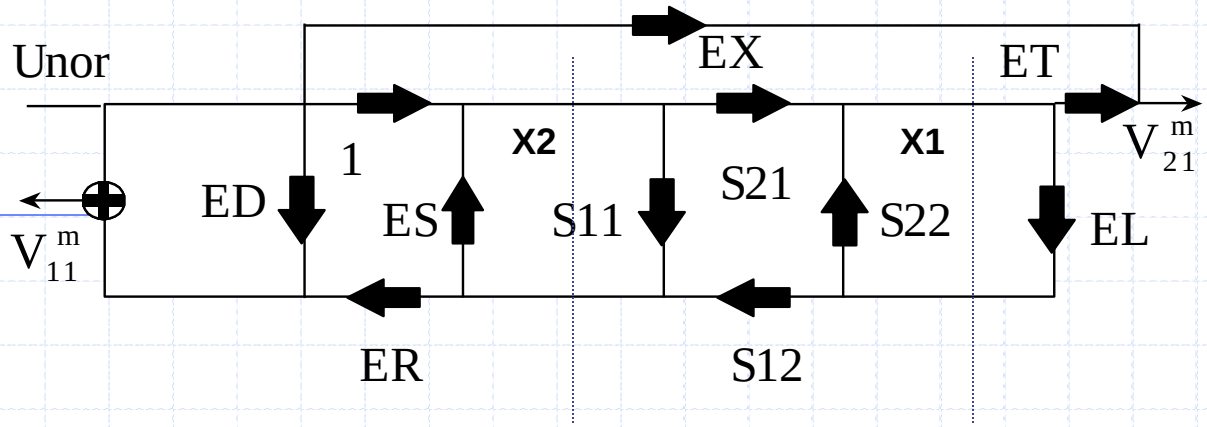
雙埠誤差模型的信號流程圖（順向和反向）



EL（the load impedance match）:負載匹配誤差

ET（the transmission frequency response）：傳輸匹配誤差

EX（the isolation）：隔離誤差



$$V_{11} = (1 + EDF) \times U_{nor} + \frac{ERF \times (S_{11} - ELF \times (S_{11} \times S_{22} - S_{21} \times S_{12}))}{1 - ESF \times S_{11} - ELF \times S_{22} + ELF \times ESF \times (S_{11} \times S_{22} - S_{21} \times S_{12})} \times U_{nor}$$

$$= EDF' + \frac{ERF' \times (S_{11} - ELF \times (S_{11} \times S_{22} - S_{21} \times S_{12}))}{1 - ESF \times S_{11} - ELF \times S_{22} + ELF \times ESF \times (S_{11} \times S_{22} - S_{21} \times S_{12})}$$

$$V_{21} = EXF \times U_{nor} + \frac{ETF \times S_{21}}{1 - ESF \times S_{11} - ELF \times S_{22} + ELF \times ESF \times (S_{11} \times S_{22} - S_{21} \times S_{12})} \times U_{nor}$$

$$= EXF' + \frac{ETF' S_{21}}{1 - ESF \times S_{11} - ELF \times S_{22} + ELF \times ESF \times (S_{11} \times S_{22} - S_{21} \times S_{12})}$$

$$EDF' = (1 + EDF) \times U_{nor}$$

$$ERF' = ERF \times U_{nor}$$

若是訊號是從順向端打入，我們此時不接待測物，而是把順向埠和反向埠都接50歐姆負載校正器，此時反向端不該有訊號，因為兩埠並沒有相接不可能有訊號，亦即透射係數 $S_{21}=0$

$$V_{21} = EXF' = EXF \times U_{nor}$$

但目前一般的機器各埠的隔離都作的蠻精確的，故隔離度誤差往往非常微小可以忽略不計。

把順向和反向埠對接，此動作稱為thru，此時對此系統反射係數S_{11}、S_{22}為零，而對於透射係數$S_{12}=S_{21}=\exp(-jw\tau_D)\approx 1$，$\tau_D$時間延遲為，而由於對接之接頭的時間延遲效應很短導致透射係數會近似於1。

$$V_{11}=(1+EDF)\times U_{nor}+\frac{ERF\times(S_{11}-ELF\times(S_{11}\times S_{22}-S_{21}\times S_{12}))}{1-ESF\times S_{11}-ELF\times S_{22}+ELF\times ESF\times(S_{11}\times S_{22}-S_{21}\times S_{12})}\times U_{nor}$$

$$=EDF'+\frac{ERF'\times(S_{11}-ELF\times(S_{11}\times S_{22}-S_{21}\times S_{12}))}{1-ESF\times S_{11}-ELF\times S_{22}+ELF\times ESF\times(S_{11}\times S_{22}-S_{21}\times S_{12})}$$

$$ELF=\frac{(V_{11}-ERF')}{ESF(V_{11}-EDF')+ERF'}$$

$$V_{21} = EXF \times U_{nor} + \frac{ETF \times S_{21}}{1 - ESF \times S_{11} - ELF \times S_{22} + ELF \times ESF \times (S_{11} \times S_{22} - S_{21} \times S_{12})} \times U_{nor}$$

$$= EXF' + \frac{ETF' S_{21}}{1 - ESF \times S_{11} - ELF \times S_{22} + ELF \times ESF \times (S_{11} \times S_{22} - S_{21} \times S_{12})}$$

$$ETF' = (V_{21} - EXF')(1 - ESF \times ELF)$$

$$ETF' = ETF \times U_{nor}$$

$$S_{11} = \left[1 + \frac{V_{22} - EDF'}{ERF'} \times ESF \times \frac{V_{11} - EDF'}{ERF' \times \Delta_F}\right] - \left[\frac{V_{21} - EXF'}{ETF'} \times \frac{V_{12} - EXF'}{ETF'} \times \frac{ELB}{\Delta_F}\right]$$

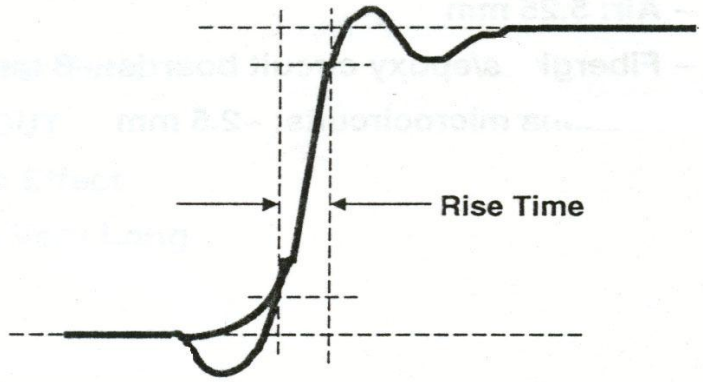
$$S_{21} = \left[1 + \frac{V_{22} - EDF'}{ERF'} \times (ESF - ELF) \times \frac{V_{21} - EXF'}{ETF' \times \Delta_F}\right]$$

$$\Delta_F = \left[1 + \frac{V_{11} - EDF'}{ERF'} \times ESF\right]\left[1 + \frac{V_{22} - EDF'}{ERF'} \times ESF\right] - \left[\frac{V_{21} - EXF'}{ETF'} \times \frac{V_{12} - EXF'}{ETF'} \times ELF^2\right]$$

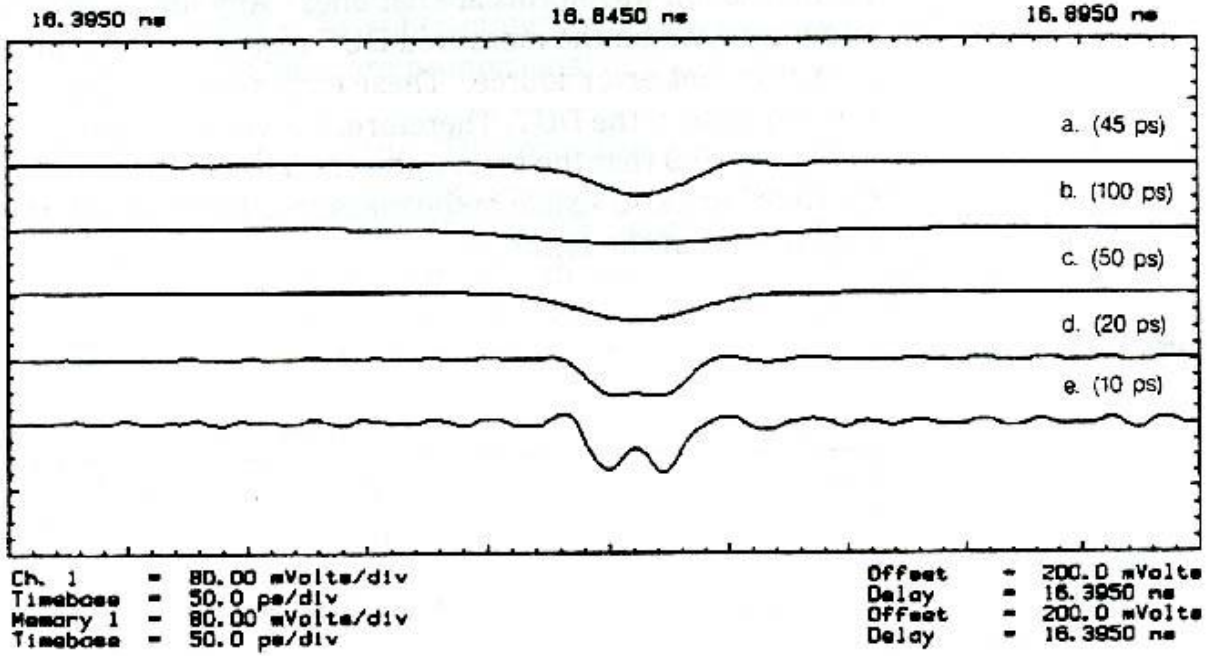
正規化(normalization)

做時域量測時除了需要作校正的動作外，往往也都需要做正規化，在此所謂的正規化亦即改變整個系統的所能看見的解析度（resolution）。

$$bandwidth = \frac{0.35}{rise\ time}$$



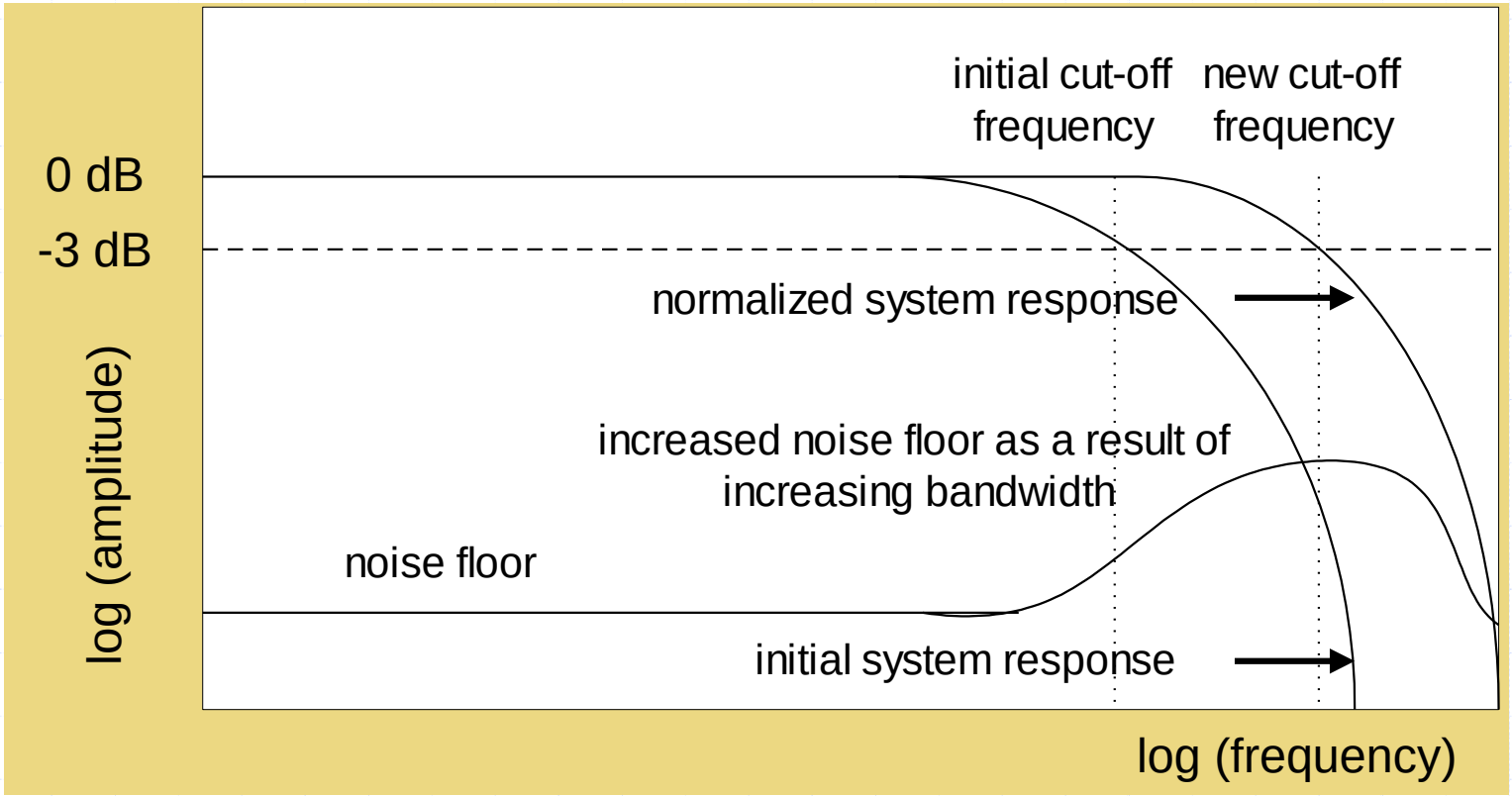
上升時間對解析度的關係圖



$$resolution = \frac{rise\ time}{2} \times V_p$$

$$V_p = \frac{V_C}{\sqrt{\varepsilon_r}}$$

正規化後之系統響應圖

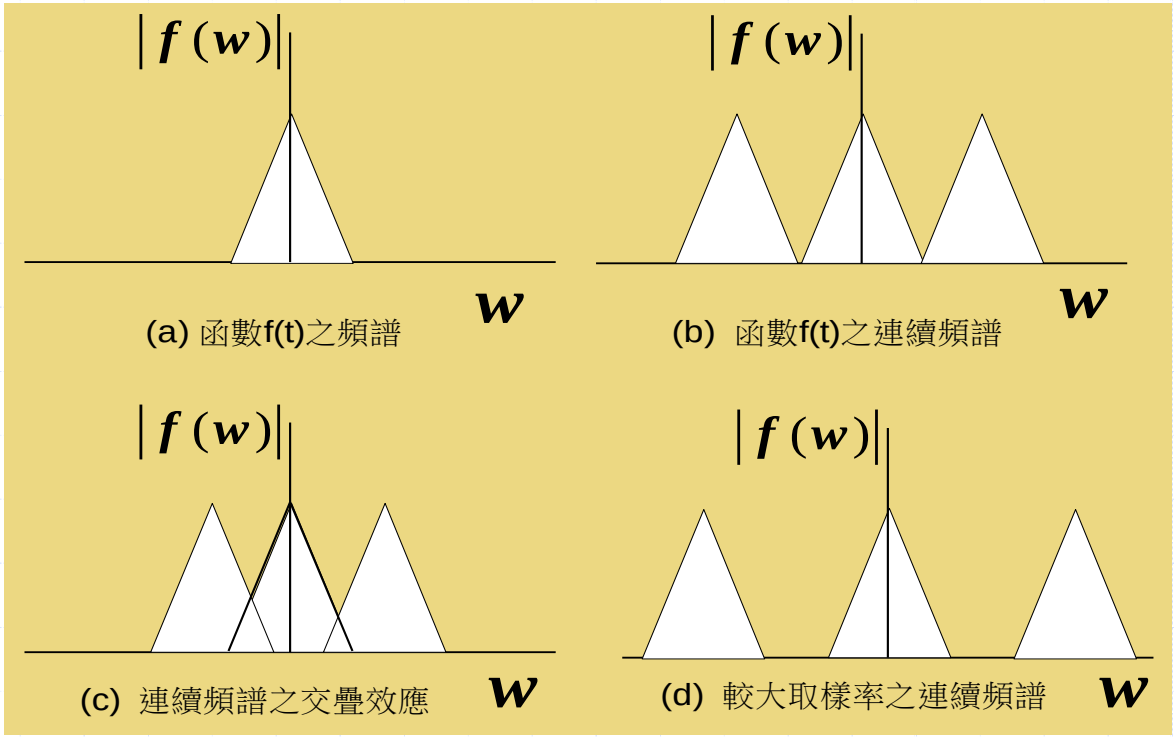

initial cut-off frequency
new cut-off frequency
0 dB
-3 dB
normalized system response
increased noise floor as a result of increasing bandwidth
noise floor
initial system response
log (amplitude)
log (frequency)

我們必須根據量測需求來作正規化。而所謂的量測需求必須根據倪奎斯取樣定理(Nyquist sampling theorem)：

$$Sampling\ Time < \frac{1}{2 \times Bandwidth}$$

擷取時域資料時若取樣週期不符合倪奎斯取樣定理，就會造成取樣時的交疊效應(aliasing effects in sampling)。

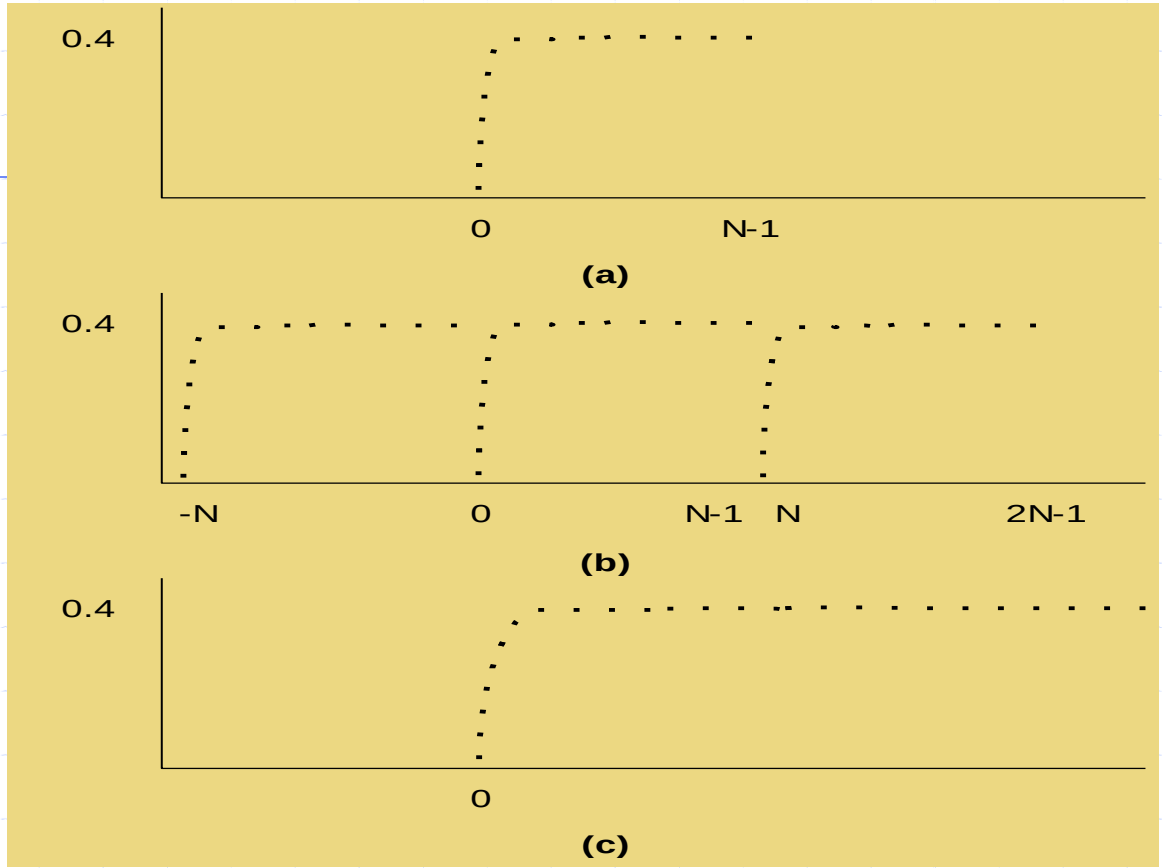
交疊效應說明圖


|f(w)|
w
(a) 函數f(t)之頻譜
|f(w)|
w
(b) 函數f(t)之連續頻譜
|f(w)|
w
(c) 連續頻譜之交疊效應
|f(w)|
w
(d) 較大取樣率之連續頻譜

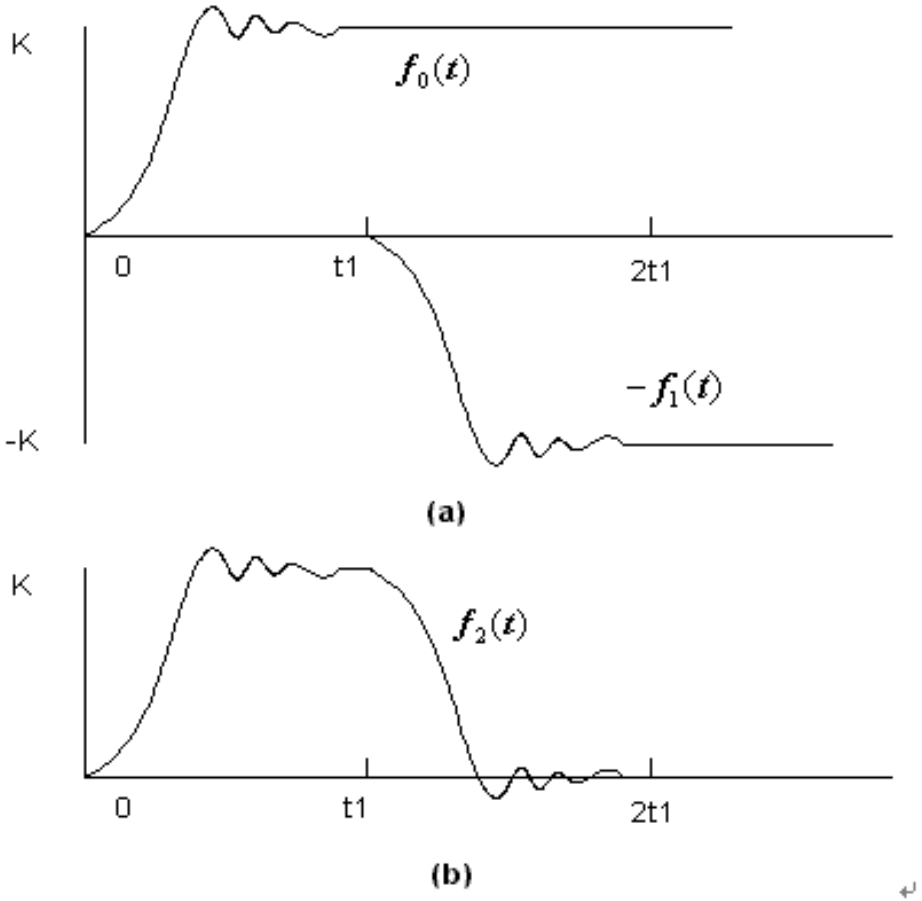
在HP_54754A(時域反射儀)中也有提供正規化的功能，然而，其正規化所能提供的上升時間取決於我們量測時的取樣時間大小

$$\min \ \text{rise time} = 8 \text{ points} \times \text{sampling time}$$

$$\max \ \text{rise time} = 50 \text{ points} \times \text{sampling time}$$



(a)量測訊號之取樣(b)週期化訊號(c)類步階信號



(a)原始信號(b)使用Gans方法變換後信號

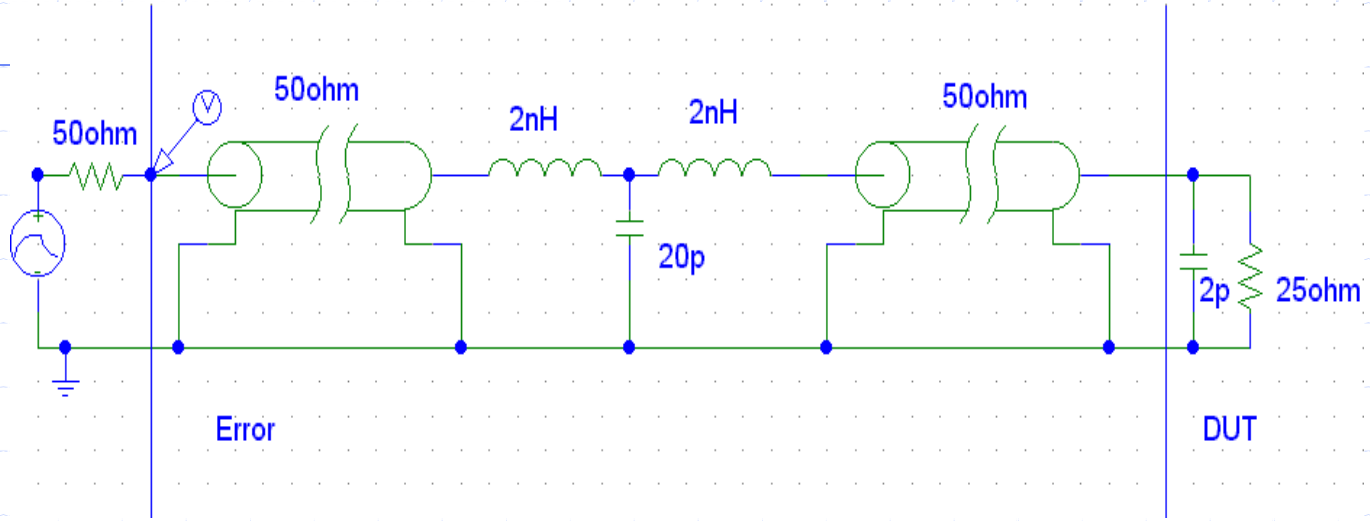
我們令要轉換的類步階函數為 $f_0(t)$ ，我們採用Gans方法變換得的函數 $f_2(t)$ ，現在我們拿來作傅立葉轉換，其推導結果如下：

$$\begin{aligned} F_2(j\omega) &= F_0(j\omega)[1-\exp(-j\omega t_1)] \\ &= F_0(j\omega)[1-(\cos\omega t_1 - j\sin\omega t_1)] \\ &= F_0(j\omega)[F_3(j\omega)] \end{aligned}$$

此時我們考慮角頻率(angular frequency) $\omega_n = n\pi / t_1$

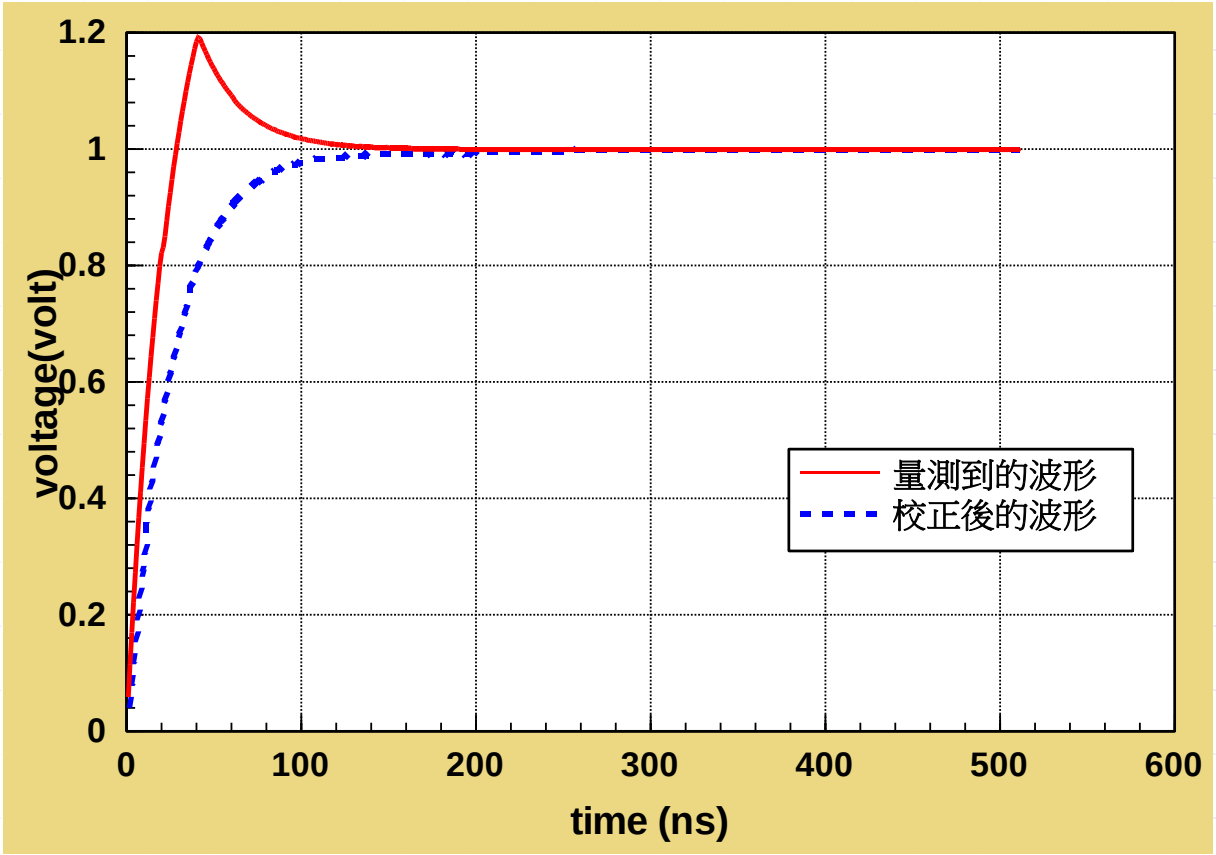
$$F_2(j\omega_n) = \begin{cases} 2F_0(j\omega_n), & \text{n}= \pm 1, \pm 3, \pm 5, \ldots \\ 0, & \text{n}= \pm 0, \pm 2, \pm 4, \ldots \end{cases}$$

單埠校正以及正規化之模擬結果

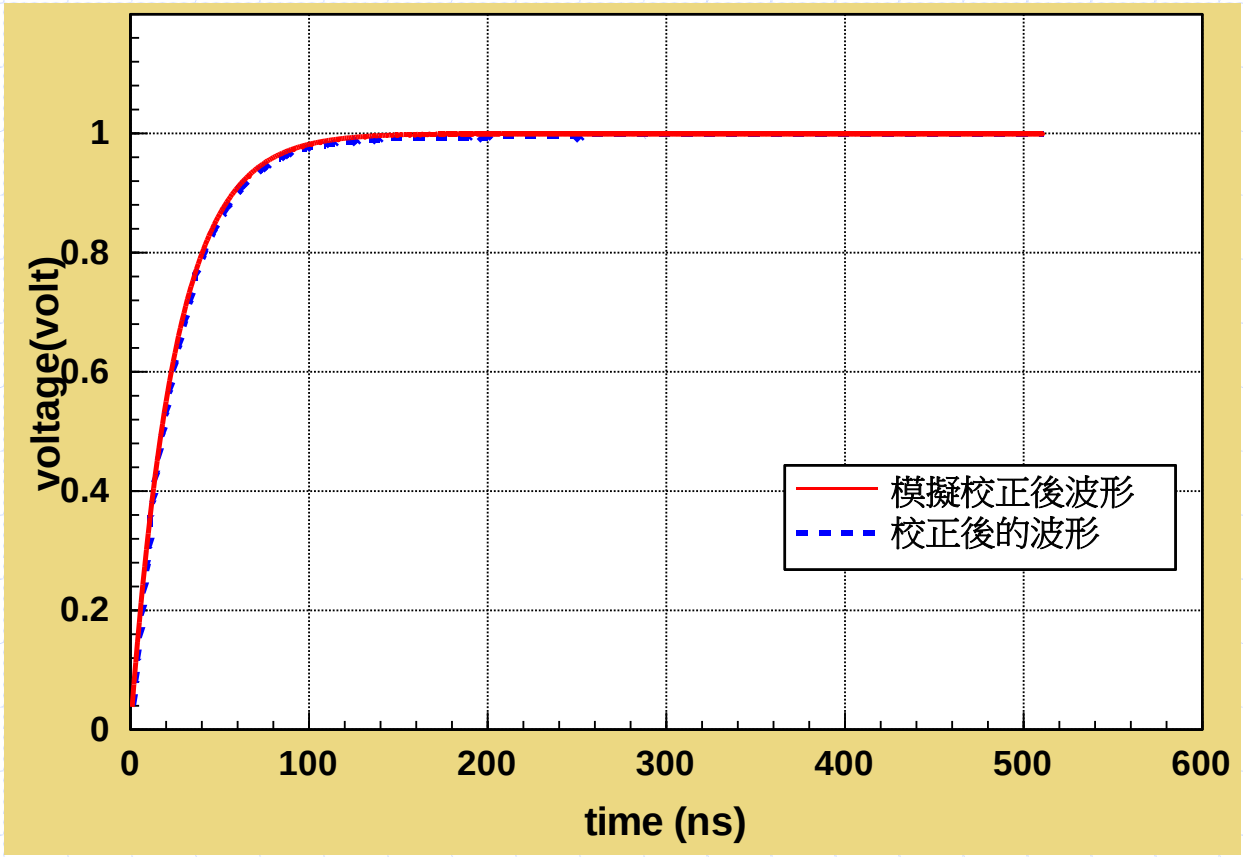


取樣時間為1ns
電壓源的上升時間為25ns
傳輸線的傳播延遲10ns

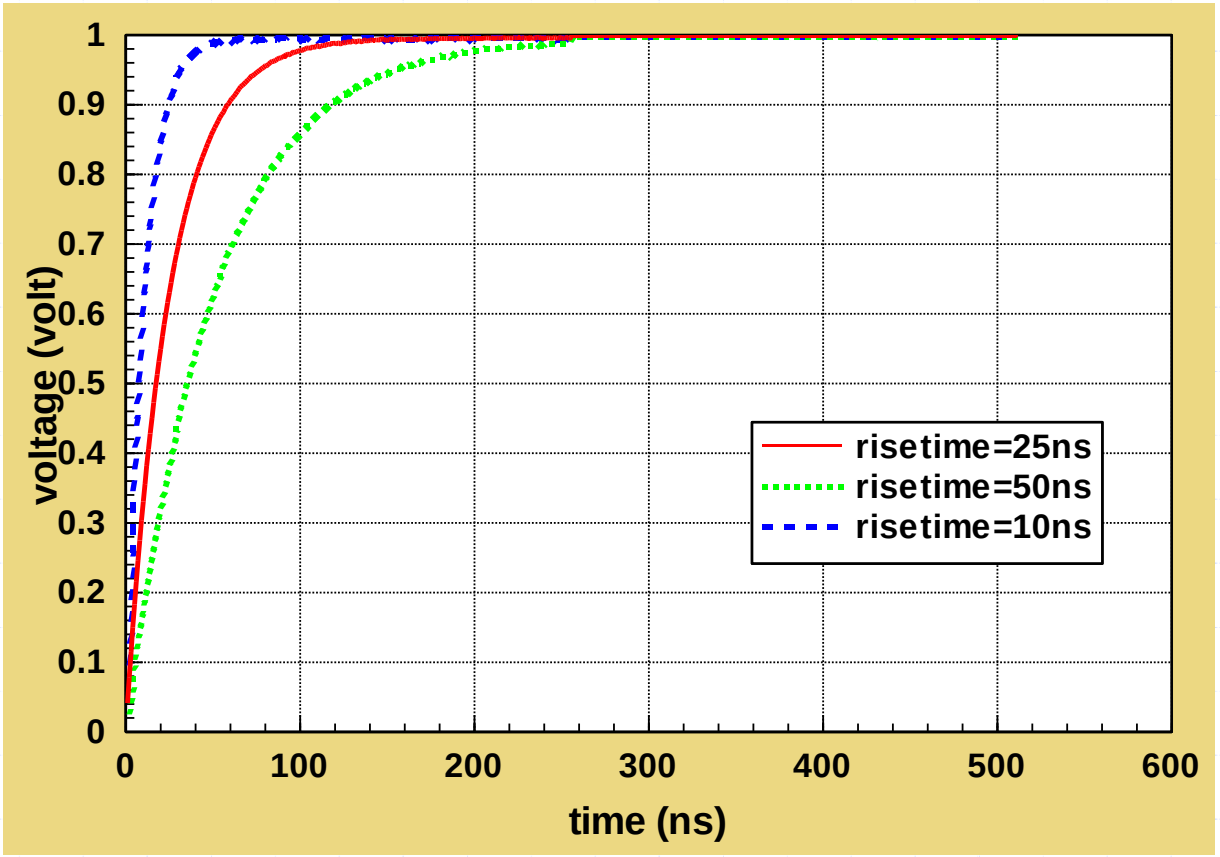
校正前後之比較


1.2
1
0.8
0.6
0.4
0.2
0
voltage(volt)
0
100
200
300
400
500
600
time (ns)
量測到的波形
校正後的波形

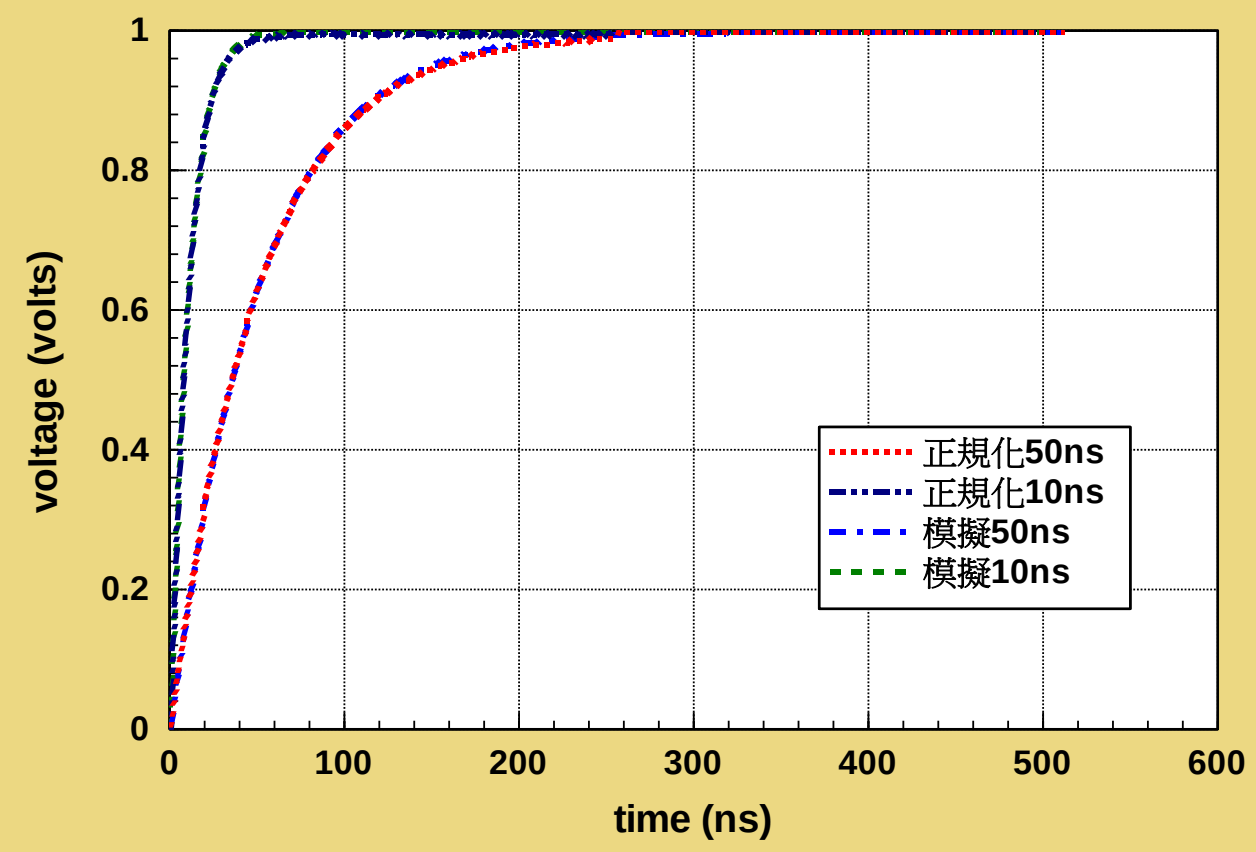
校正後與模擬理想狀況之比較



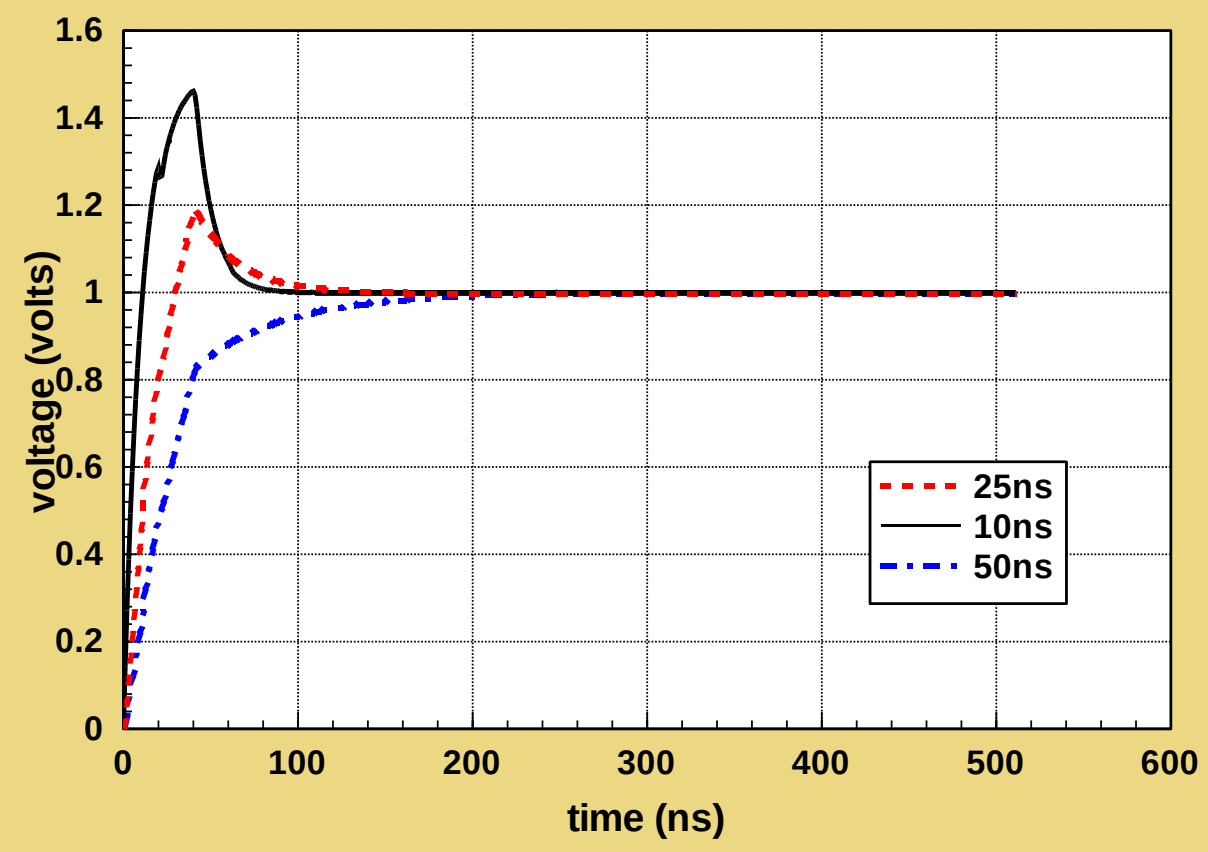
正規化後之結果


voltage (volt)
time (ns)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
100
200
300
400
500
600
risetime=25ns
risetime=50ns
risetime=10ns

正規化後結果和模擬比較



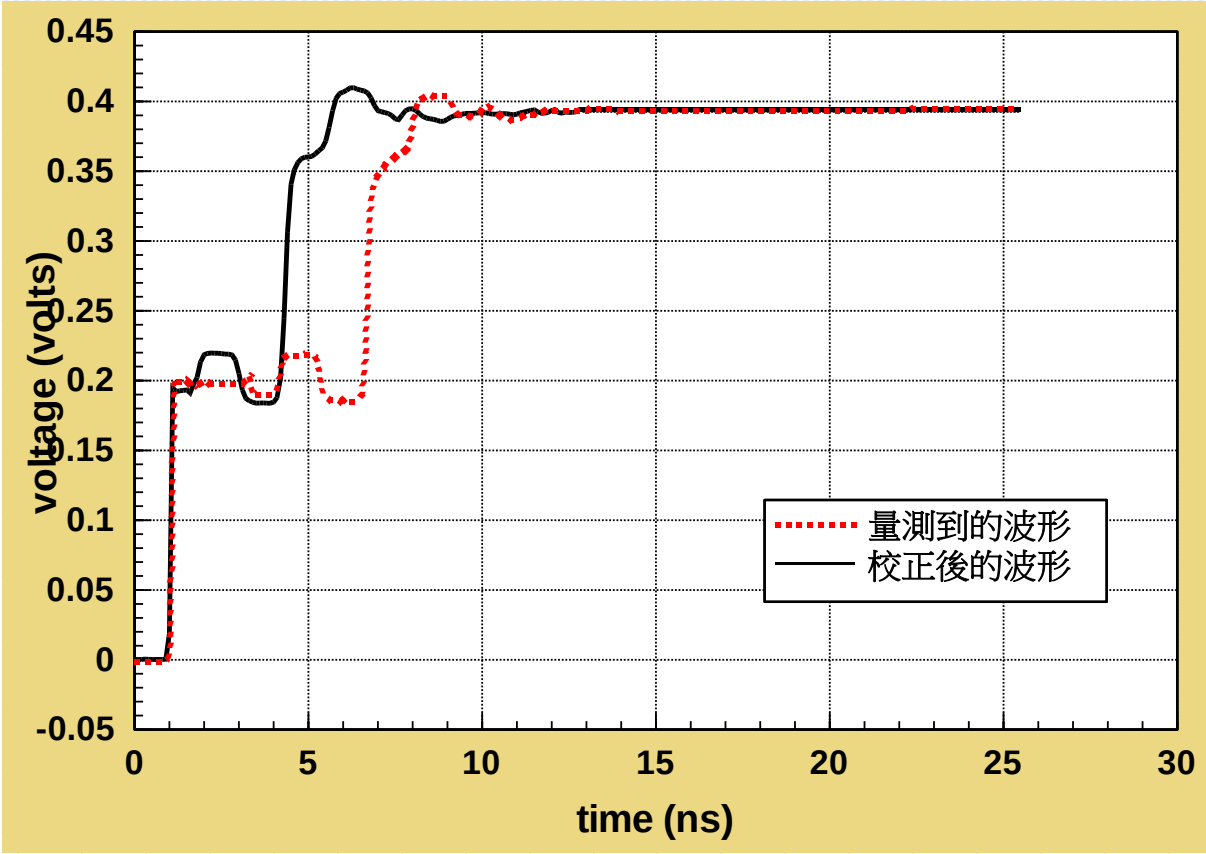
上升時間對解析度的影響



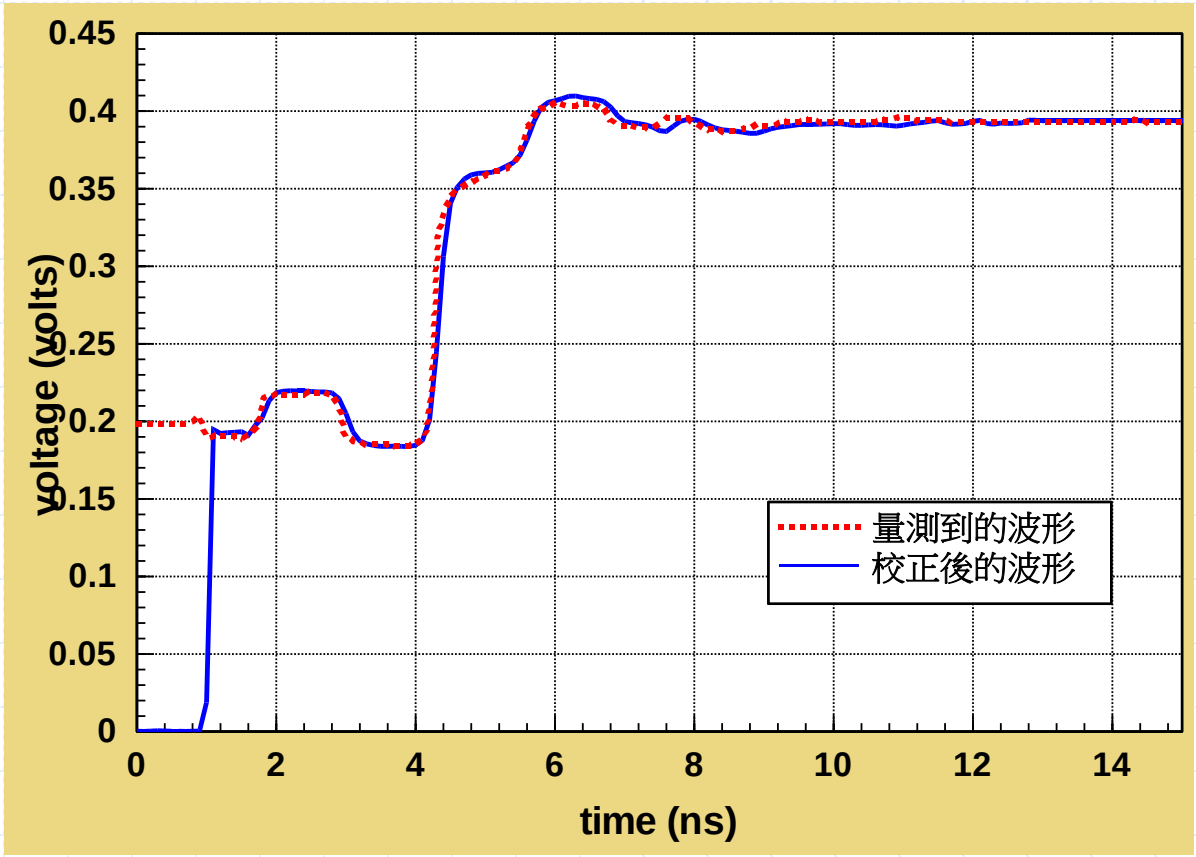
單埠校正以及正規化之實際量測結果

取樣時間是100 ps
入射波的上升時間為50 ps
HP同軸饋入線長度約為2.2 ns
量測系統是採用HP54754A的TDR模組
加上HP54750示波器

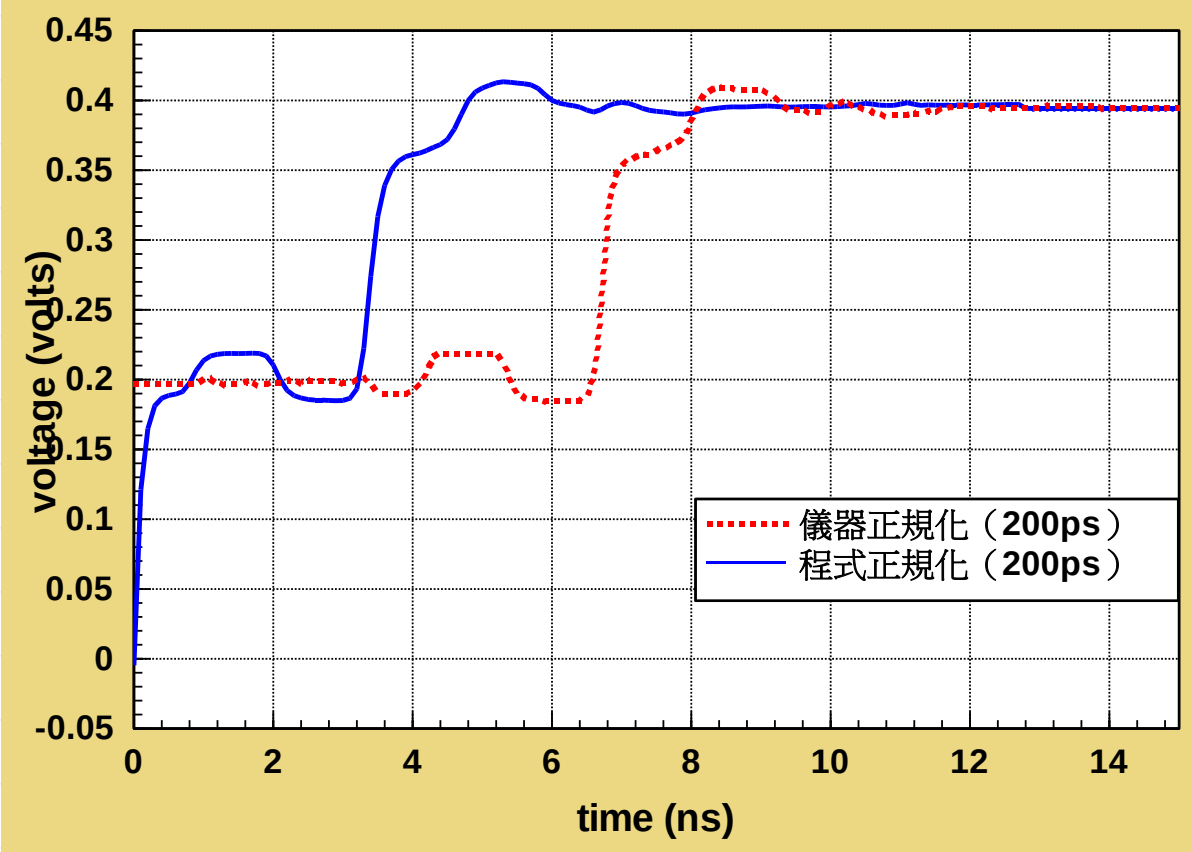
校正前後之比較


0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
-0.05
voltage (volts)
0
5
10
15
20
25
30
time (ns)
量測到的波形
校正後的波形

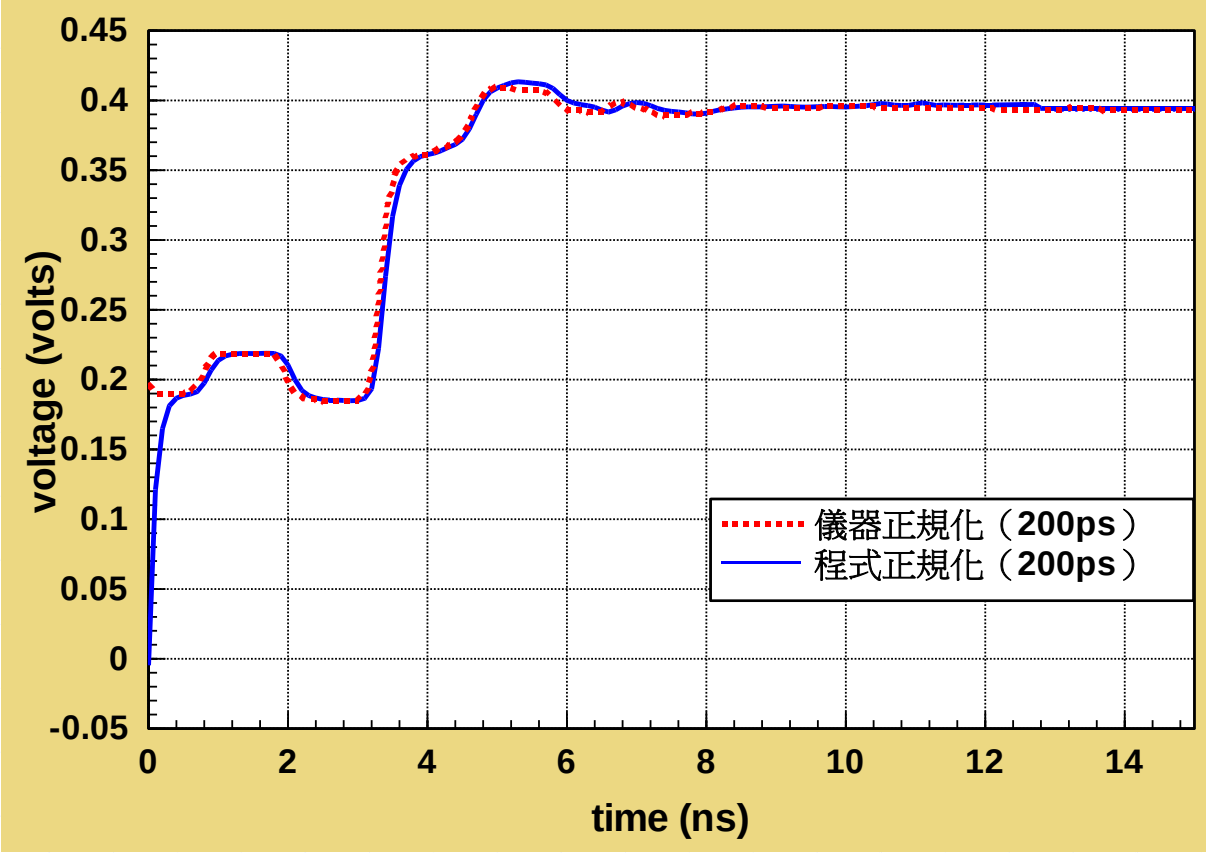
校正前後的波形重疊比較



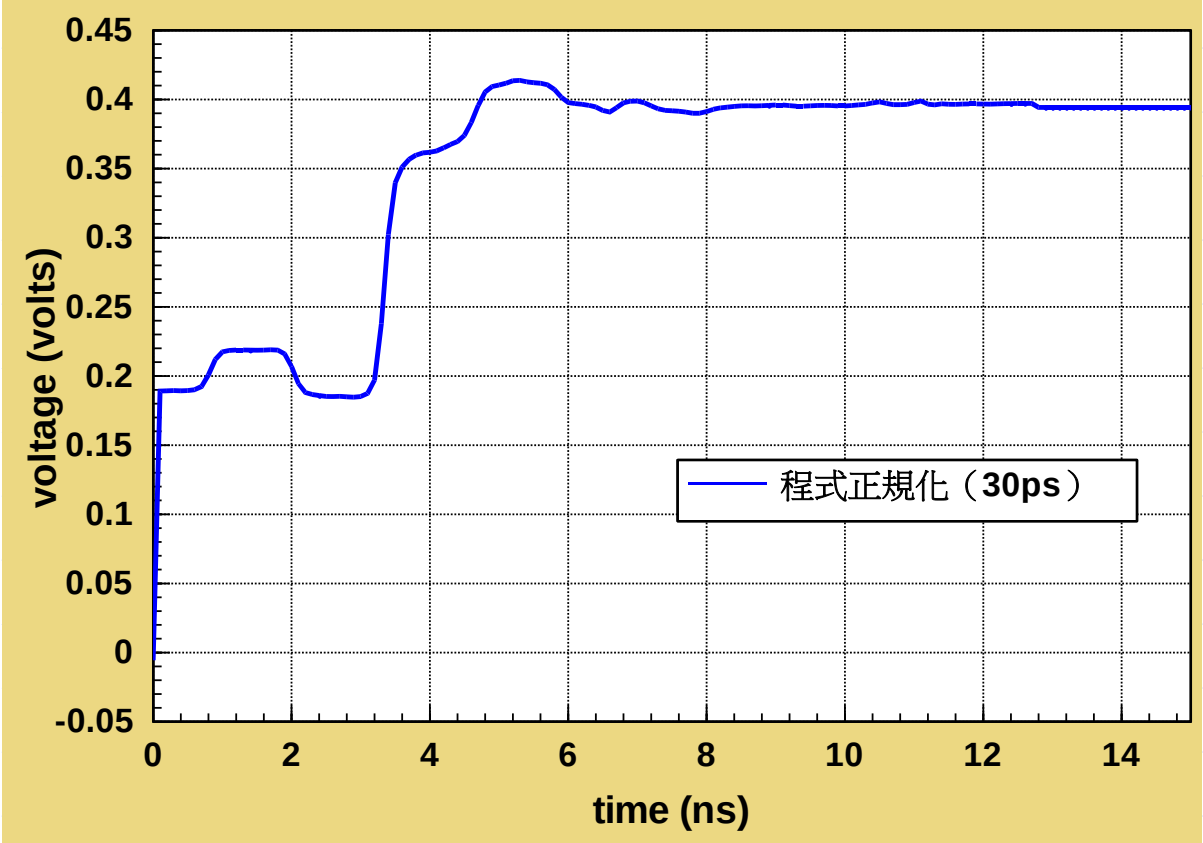
儀器正規化和自撰程式正規化比較



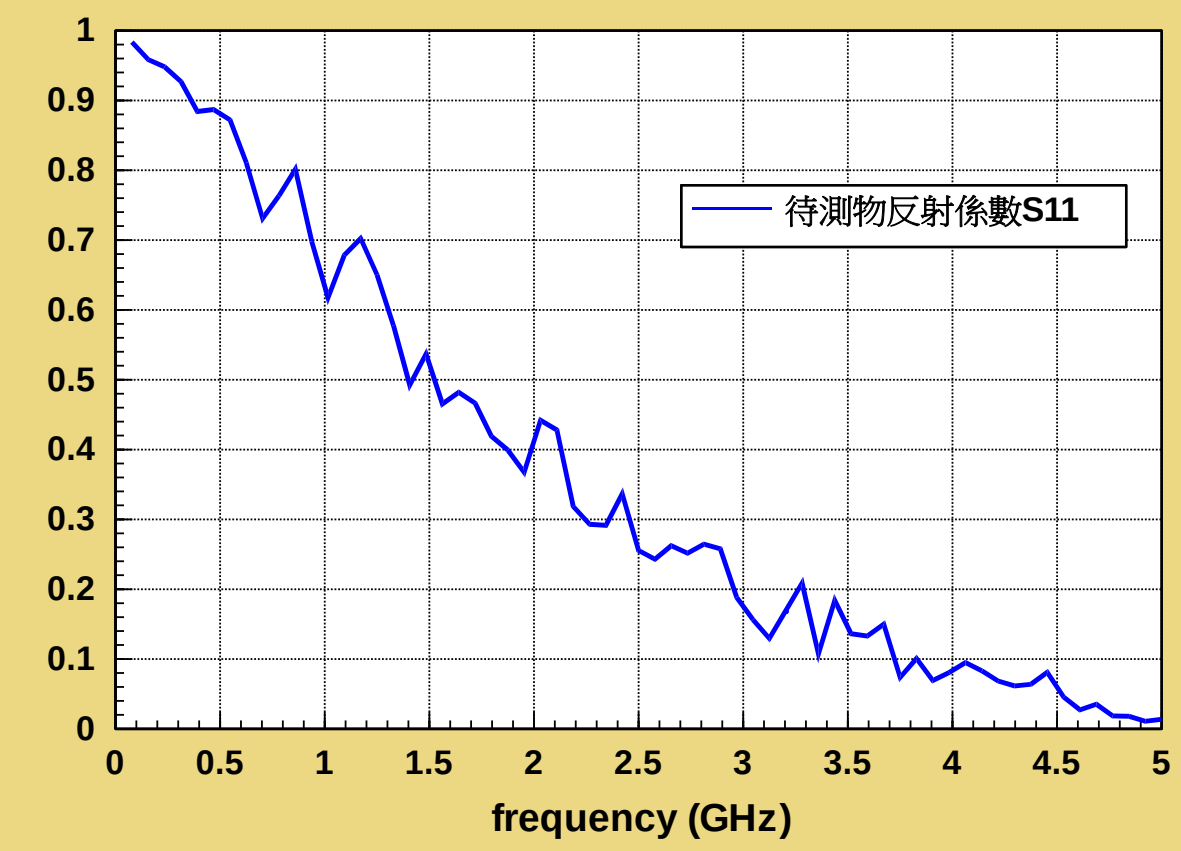
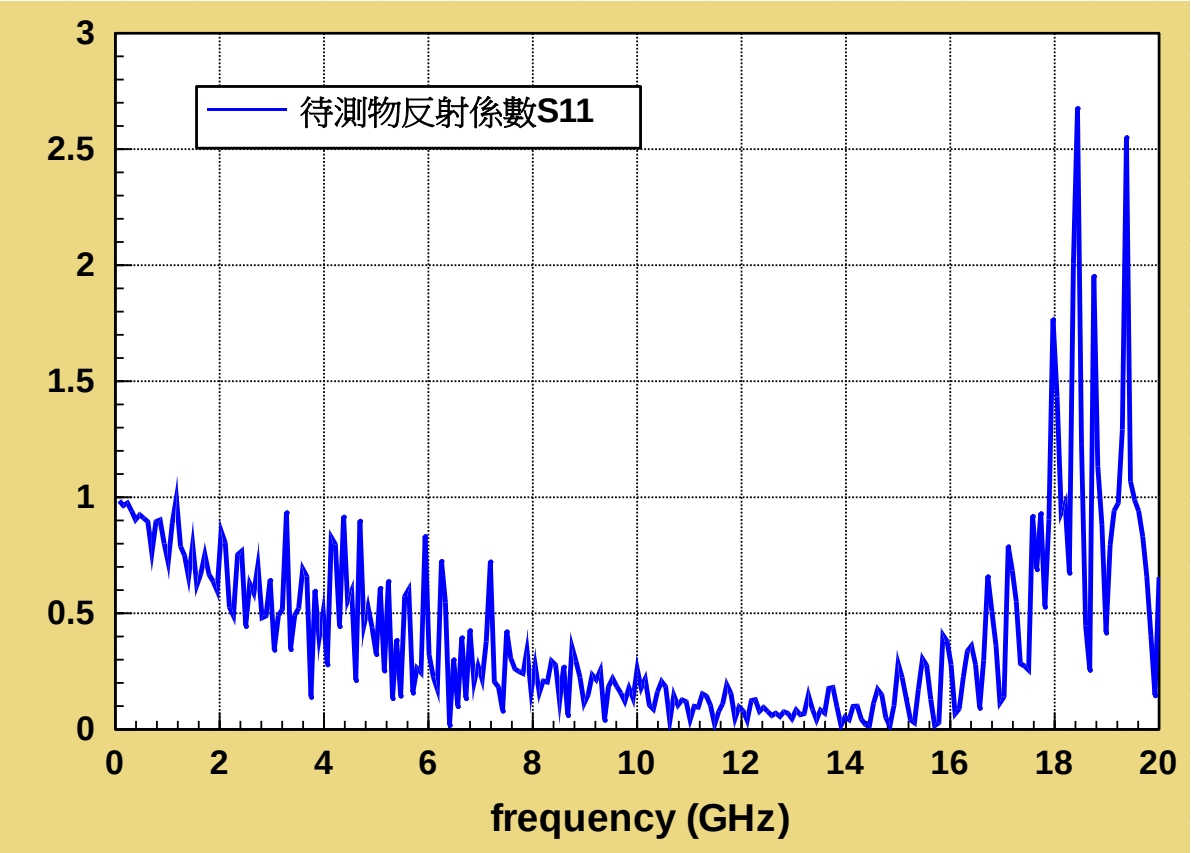
儀器和自撰程式正規化比較（重疊後）



自撰程式正規化(30ps)



校正後待測物反射係數


1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
frequency (GHz)
待測物反射係數S11

當取樣時間減為25ps時之校正後待測物反射係數出現計算上的高頻誤差