EMC Considerations for DC Power Design

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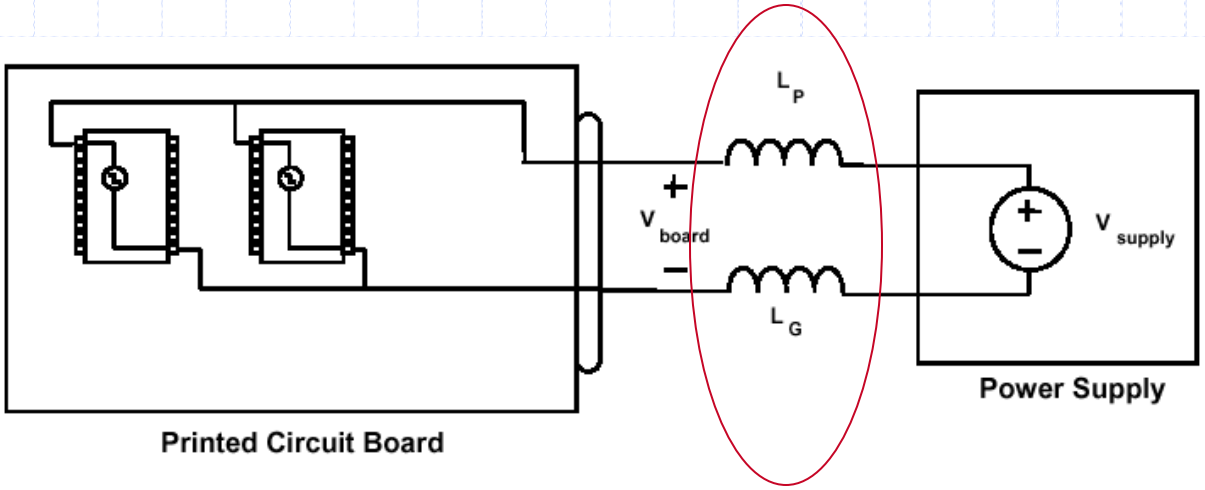
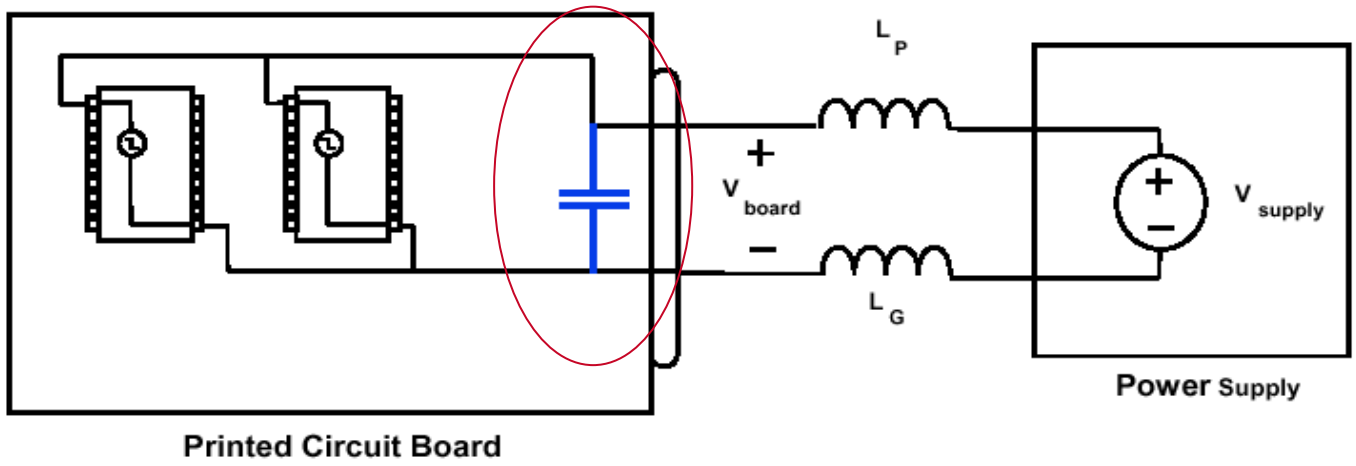
Power Bus Noise below 5MHz



Power Distribution Model ~ (0 - 5 MHz)

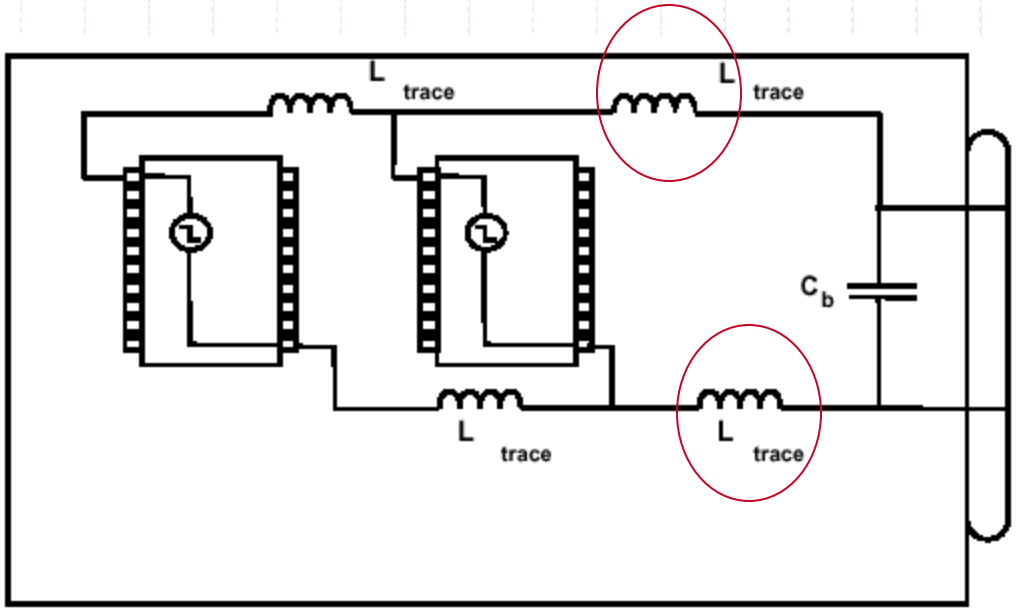
Power Bus Noise below 5MHz (Solution)

Add Bulk capacitance



Power Distribution Model ~ (0 - 5 MHz)

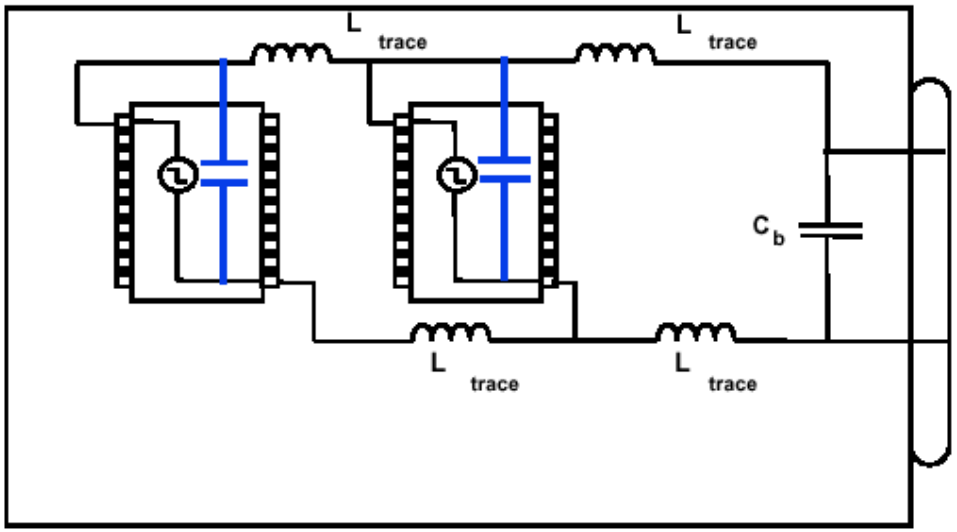
Power Bus Noise between 5MHz to 50MHz



Power Distribution Model ~ (5 - 50 MHz)

Board without power and ground planes

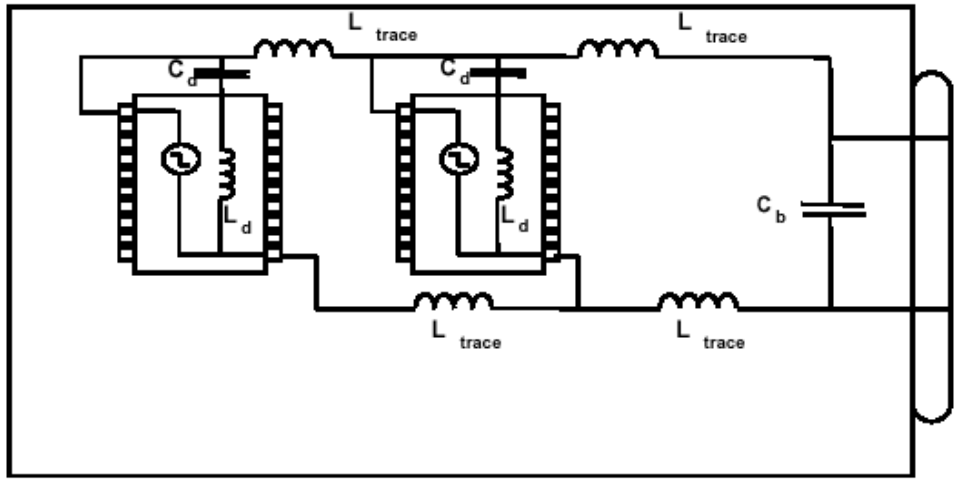
Power Bus Noise between 5MHz to 50MHz (Solution)



Power Distribution Model ~ (5 - 50 MHz)

Board without power and ground planes

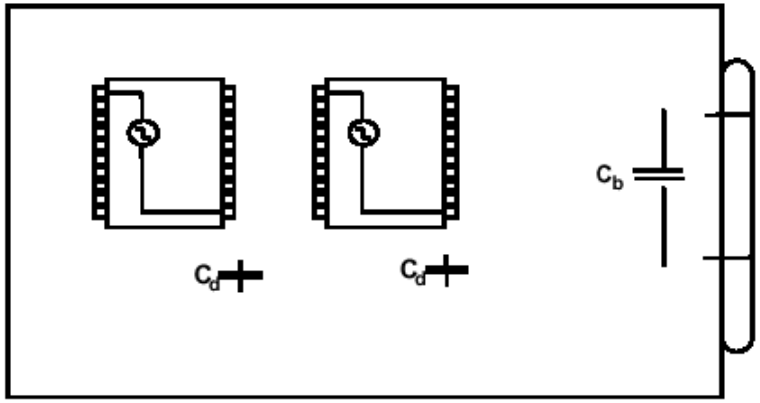
Power Bus Noise between 50MHz to 500MHz



Power Distribution Model ~ (50 - 500 MHz)

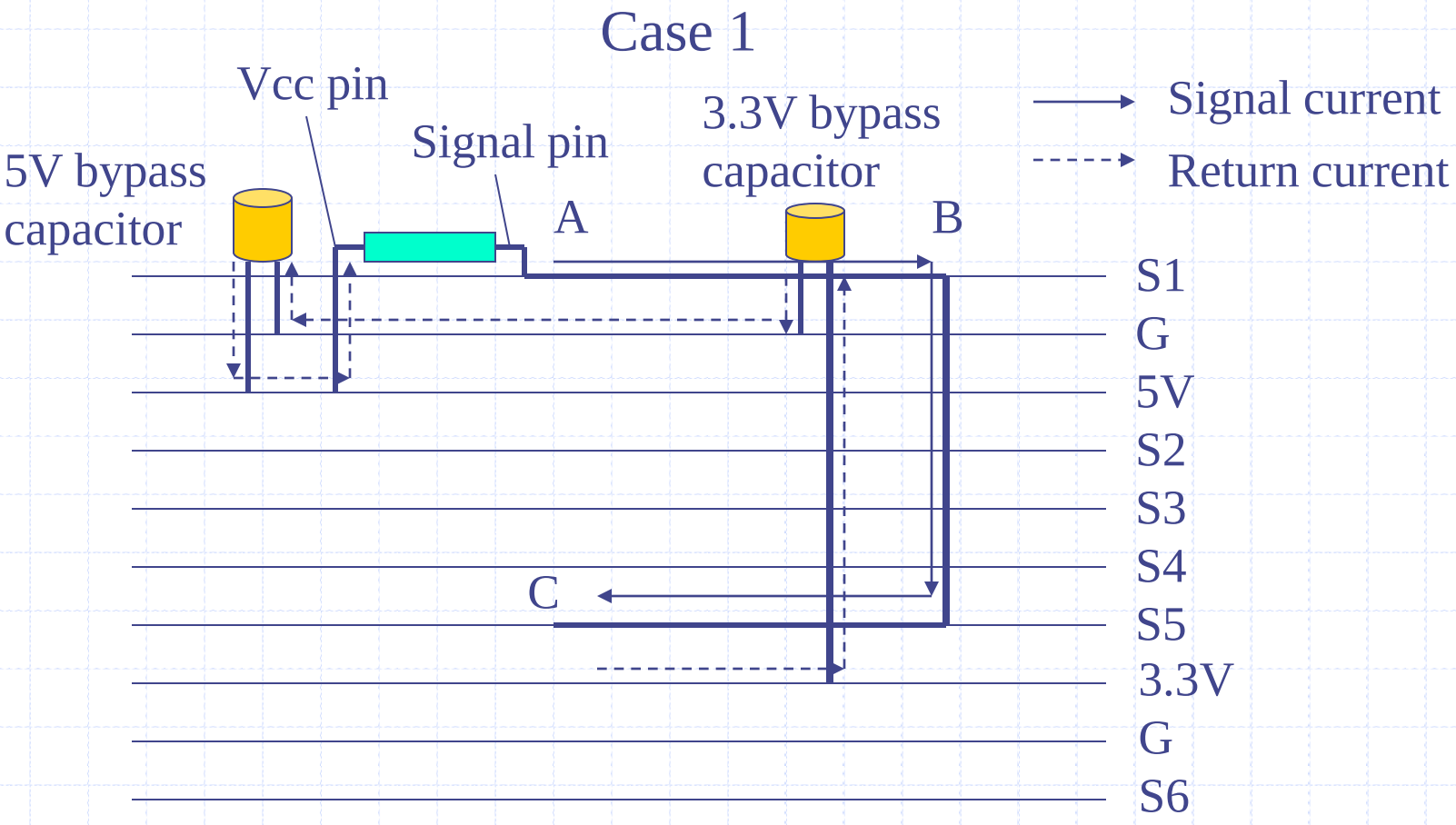
Board without power and ground planes

Power Bus Noise between 50MHz to 500MHz (Solution)



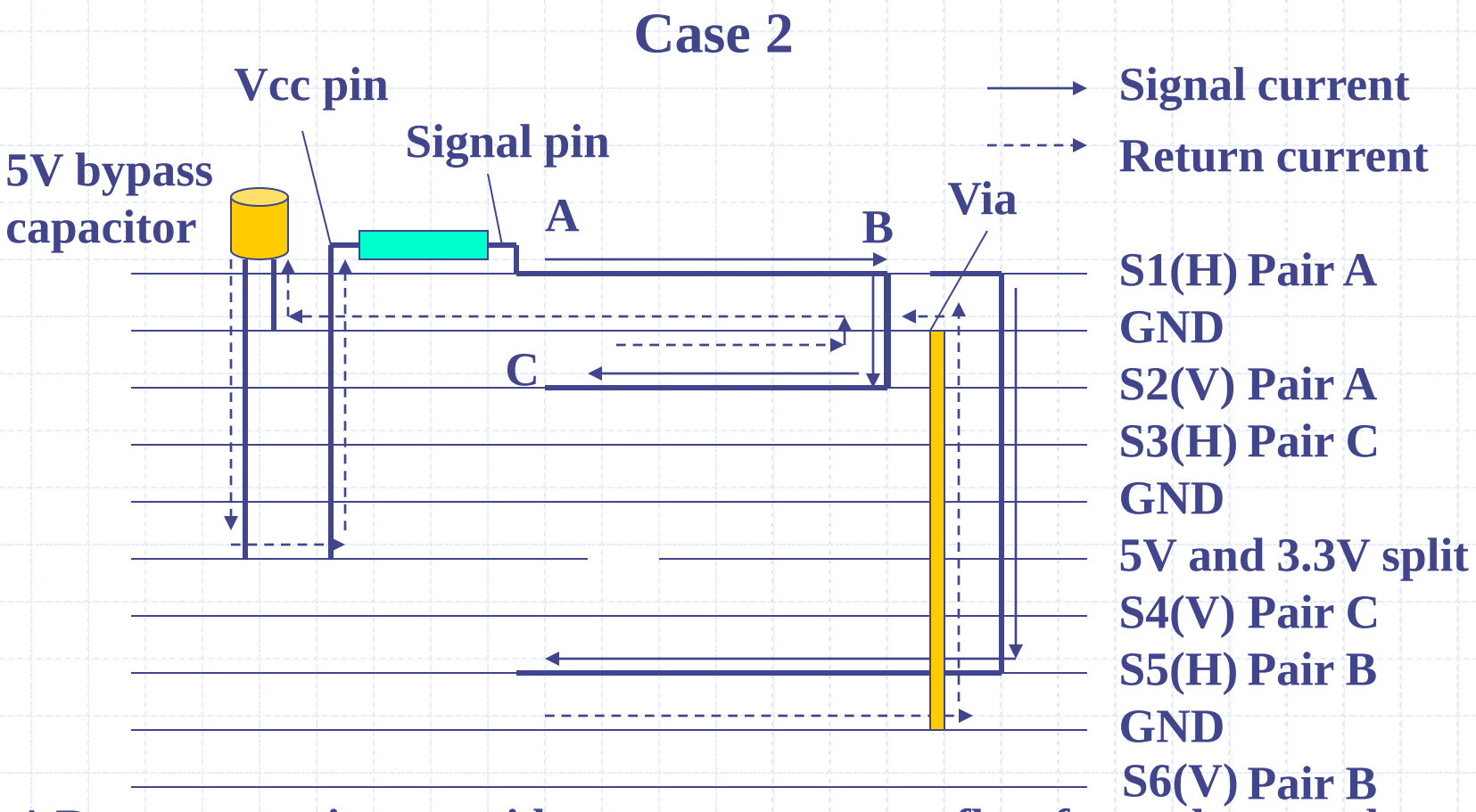
Power Distribution Model ~ (5 - 500 MHz)
Board with power and ground planes

RF Path in power bus (I)



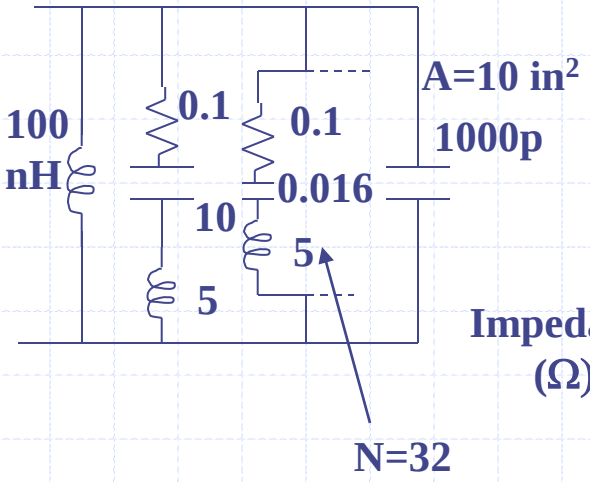
* Bypass capacitor provide return currents to flow from plane to plane

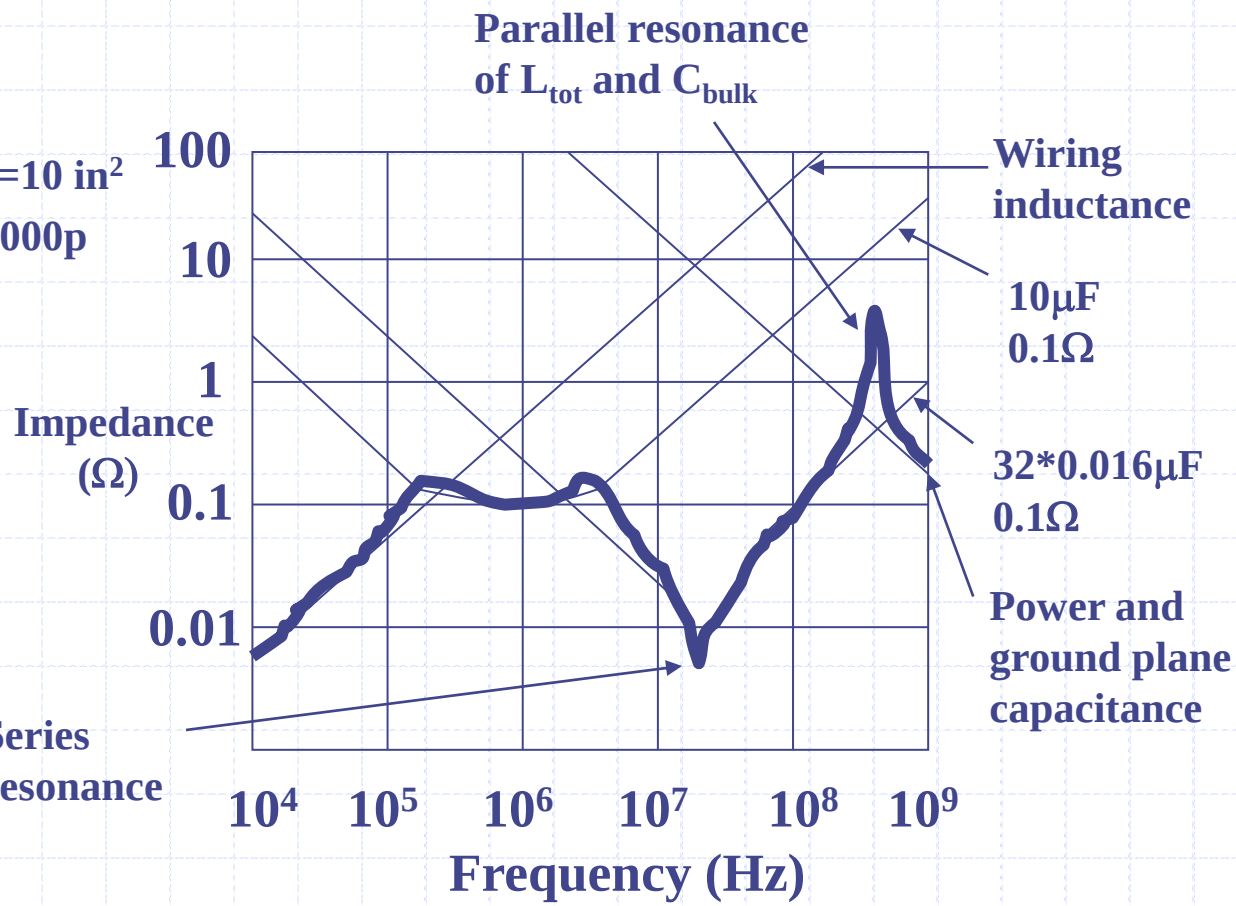
RF Path in power bus (II)



* Bypass capacitor provide return currents to flow from plane to plane

A simple power bus model





Power Bus Impedance

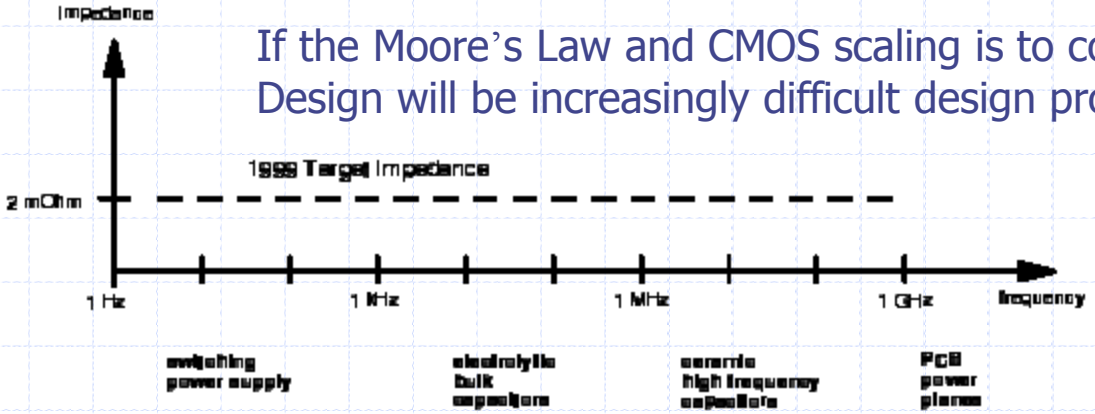
TABLE I
TARGET IMPEDANCE IS DROPPING BY A FACTOR OF 5 EVERY COMPUTER GENERATION

year	voltage (volts)	power dissipated (watts)	current (amps)	Ztarget (mOhms)	frequency (MHz)
1990	5.0	5	1	250	16
1993	3.3	10	3	54	66
1996	2.5	30	12	10	200
1999	1.8	90	50	1.8	600
2002	1.2	180	150	0.4	1200

$$Z_{\text{target}} = \frac{(\text{Power Supply Voltage}) \times (\text{allowed ripple})}{\text{current}}$$
$$= \frac{(5\ \text{V}) \times (5\%)}{1\ \text{A}} = 0.250\ \text{Ohms.}$$

Power Bus Impedance (an example)

If the Moore's Law and CMOS scaling is to continue, the power bus Design will be increasingly difficult design problems.



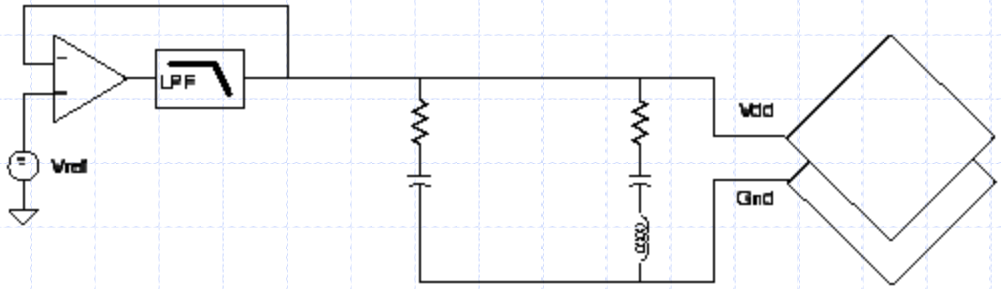
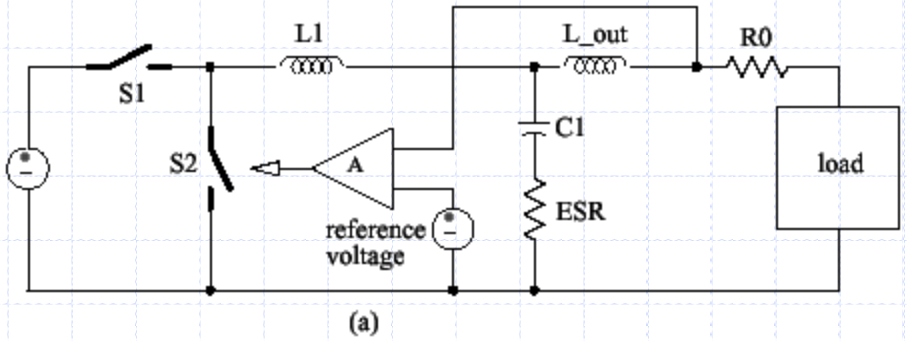


Figure 1: A flat power supply impedance vs. frequency is met by using VRM, bulk capacitor, high frequency ceramic capacitor and power plane components.

Voltage Regulator Module (VRM)

- The VRM converts one DC voltage to another, for example 5V to 1.8V.
- It has a reference voltage and a feedback loop.
- The bandwidth of the regulation loop is usually between 1kHz to several hundred kHz.
- At frequencies above the loop bandwidth, the VRM becomes high impedance.

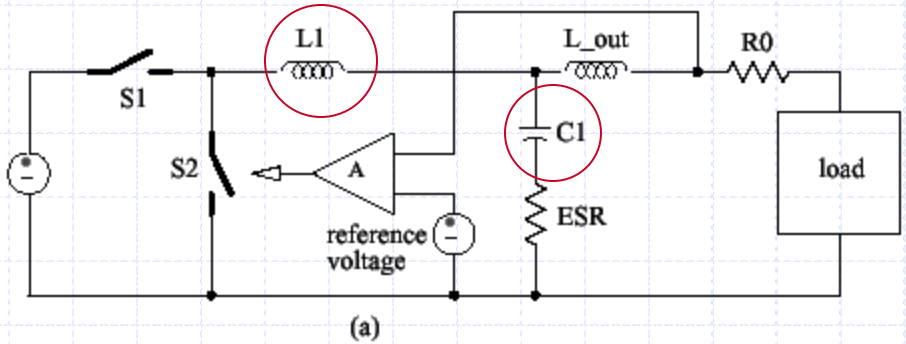


(a)

Voltage Regulator Module (VRM) : working mechanism

Inductor

1. S1 close, S2 open : load is demanding current, L1 is storing energy.
2. If L1 supply more current than the load demanding, S1 open, S2 close.
3. Current continues to flow to the load until S2 opens, S1 closes again.



Capacitor

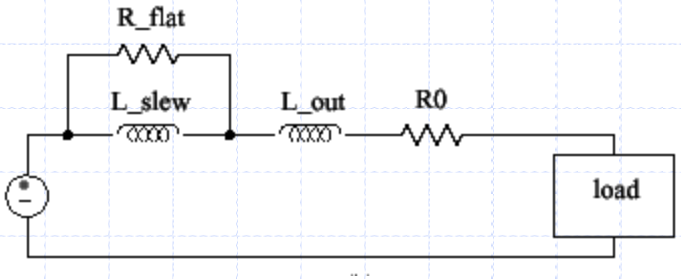
C1 smoothes out the voltage.

Amplifier A

1. When the load voltage is too low, it causes the switches and inductor to ramp up the current.
2. When the load voltage is too high, it causes the switches and inductor to ramp down the current.

Voltage Regulator Module (VRM) : linear model

1. The buck regulator is nonlinear because switches open and closed as a function of time.
2. A linear model of VRM is necessary in the design phase of the Power Bus.
3. The linear model below is accurate enough to estimate the amount of the bulk capacitance.



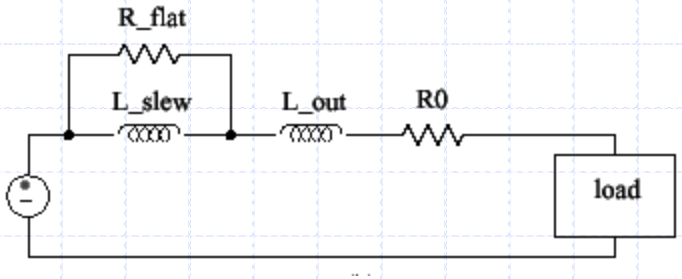
1. R0 is the value of the resistor between VRM sense point and the actual load.
2. L_out is the output inductance
   - It may be the cables that connect the VRM to the system board (200nH)
   - Or the inductance of the pins connecting the VRM to the CPU module (4nH)
3. R_flat is the ESR of the capacitor associated with the VRM.
4. **What is the L_slew and its value ?**

Voltage Regulator Module (VRM) : linear model

1. L_slew is the only element in the linear model that is not traceable back to an element in the nonlinear VRM model.
2. The value of L_slew is chosen so that current will be ramped up in the linear model in about the same time that it is ramped up in a real VRM.

For example

$$L\_slew = V\frac{dt}{di} = (1.8V * 0.05)\frac{15uSec}{20A} = 67.5nH$$

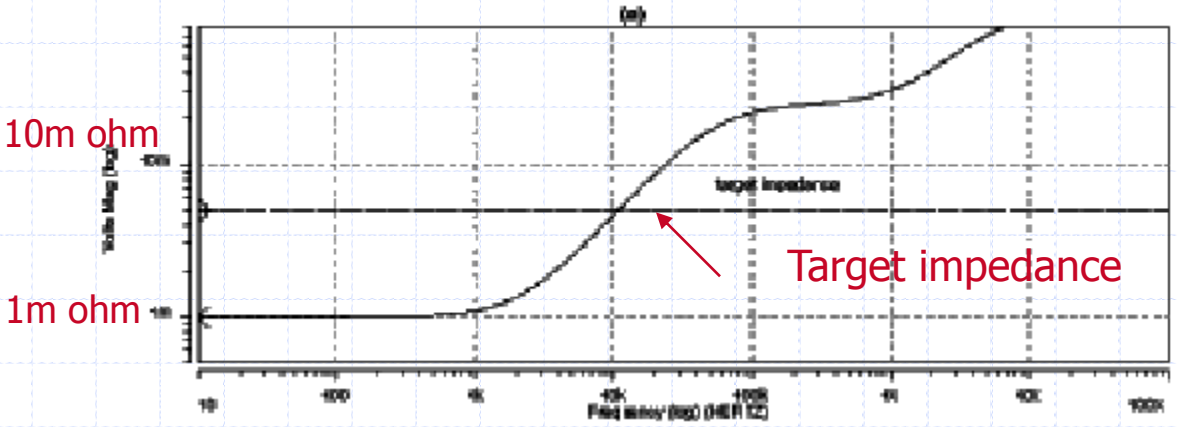


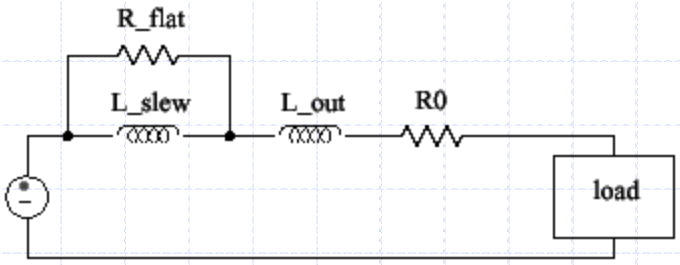
Typical parameters for a VRM attached on a processor module

parameter	value	units
R0	1	mOhm
L_out	4	nH
R_flat	30	mOhms
L_Slew	67.5	nH

VRM : behavior example

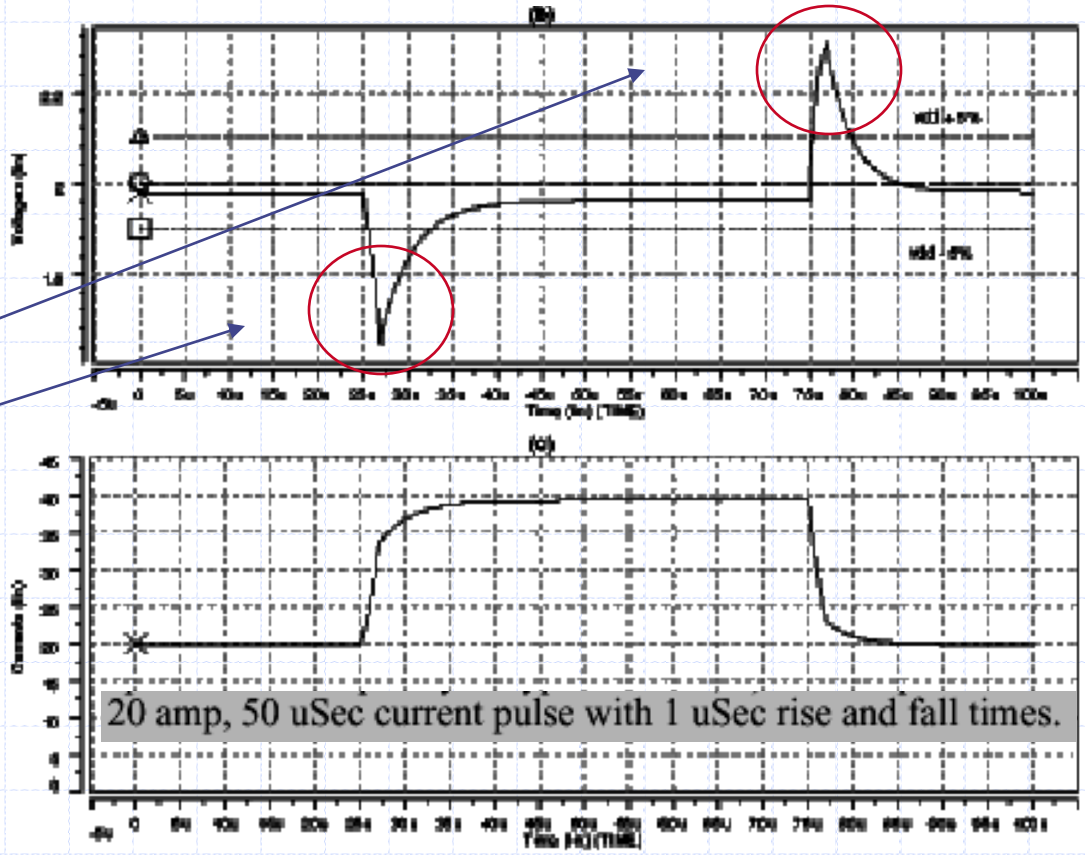
Impedance V.S. Frequency





VRM : behavior example

VRM voltage v.s. time transient



Over spec. Why ?

Bulk Capacitance

Bulk capacitors are necessary to maintain the power bus impedance at frequencies above those maintained by the VRM and below the frequencies where ceramic capacitors are effective.

The capacitance value can be roughly estimated by

$$C = I\frac{\Delta t}{\Delta V}$$

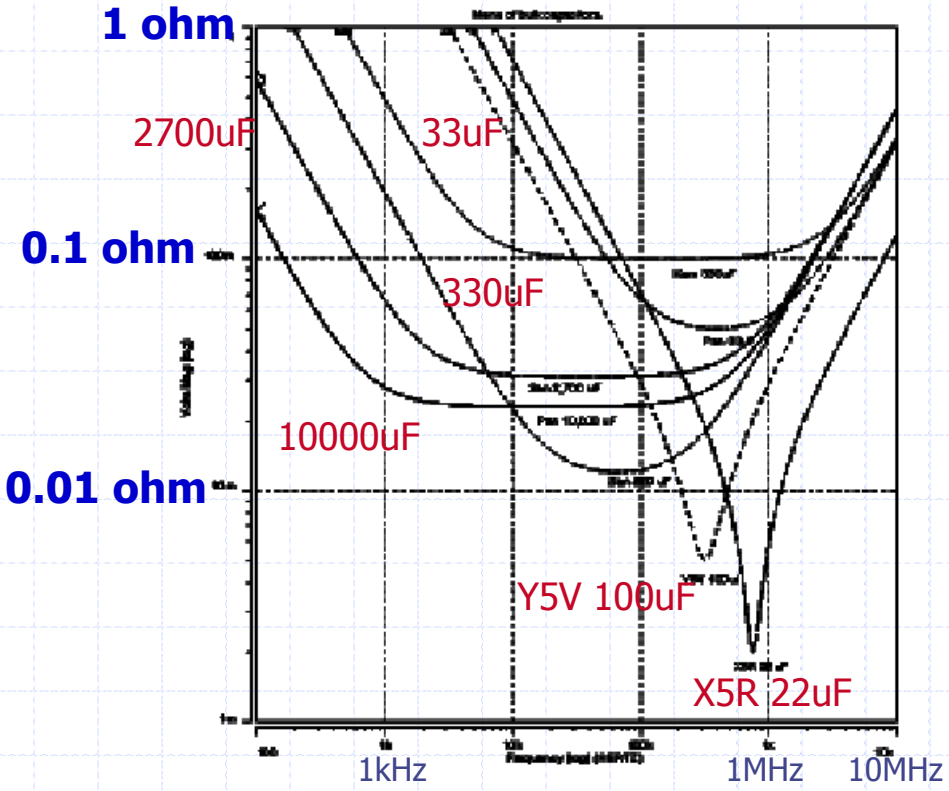
Ex: For 20A current transient, the VRM responds in 15us, and the PDS should remain in 5% of 1.8V.

$$C = I\frac{dt}{dv} = 20\,\mathrm{A} * \frac{15\mu s}{1.8\,\mathrm{V} * 0.05} = 3333\ \mu\mathrm{F}.$$

Does the capacitance value enough or over ?

Bulk Capacitance: frequency response

A: This estimation maybe overestimate the required bulk capacitance by a factor 2 because The VRM is ramping up current and the average current may be half of the final value during the VRM response time.

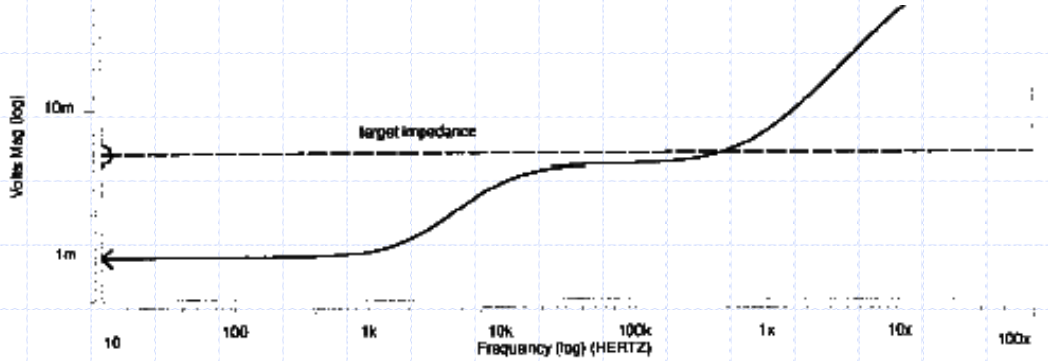


Bulk capacitance can be modeled by the **series of RLC**

Bulk Capacitance: behavior

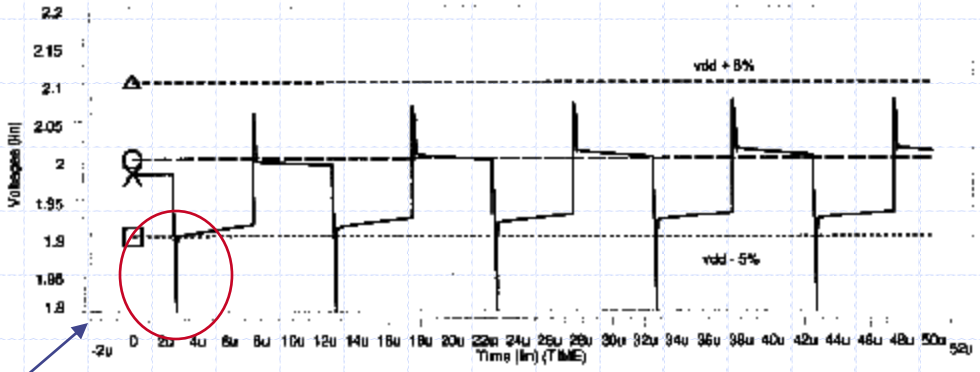
Output impedance v.s. frequency when a VRM is placed in parallel with 5 x 2700uF electrolytic bulk capacitance

The impedance is under spec up to almost 1MHz



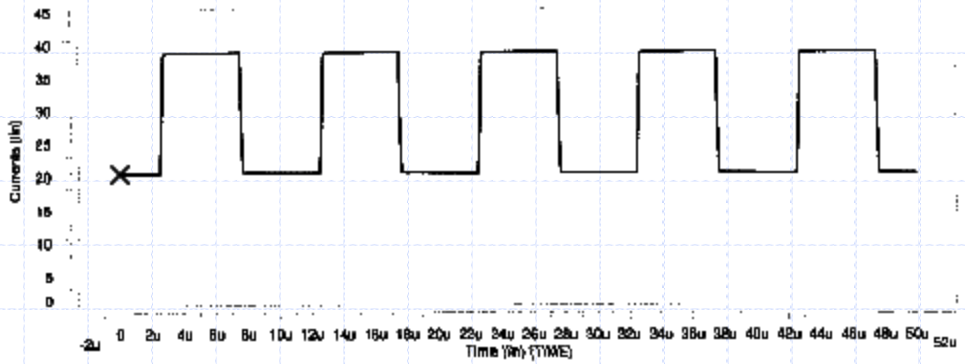
Bulk Capacitance: behavior

20A current transients at 100kHz with 200ns rise/fall time



(b)

Over spec (5%), why ?



High Frequency Ceramic Capacitance: Type

Dielectric type	ESR	Reliability	Value
NPO	lowest	best	Up to a few nF
X7R	dependent	good	Several nf to several uF
X5R	dependent	fair	Several nF to 100 uF
Y5V	dependent	Poor	High capacitance

Package size:
0603
1206
0805

High Frequency Ceramic Capacitance: Model

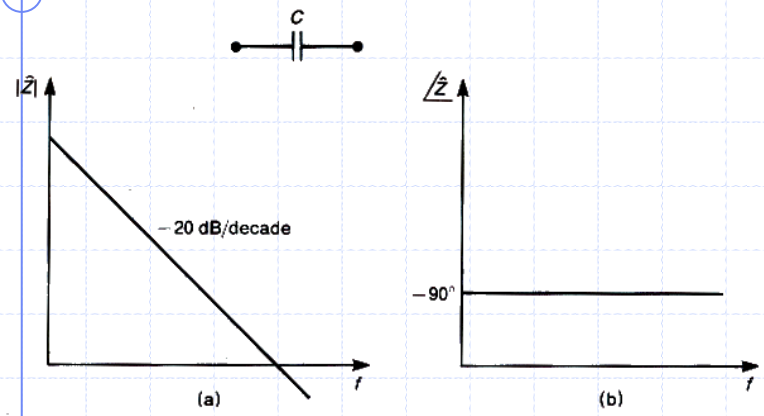


FIGURE 6.22 Frequency response of the impedance of an ideal capacitor: (a) magnitude; (b) phase.

Ideal model

real model

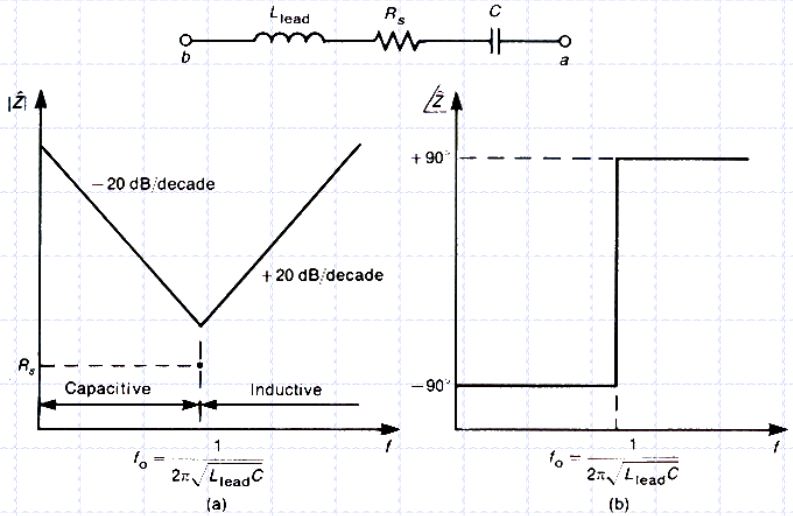
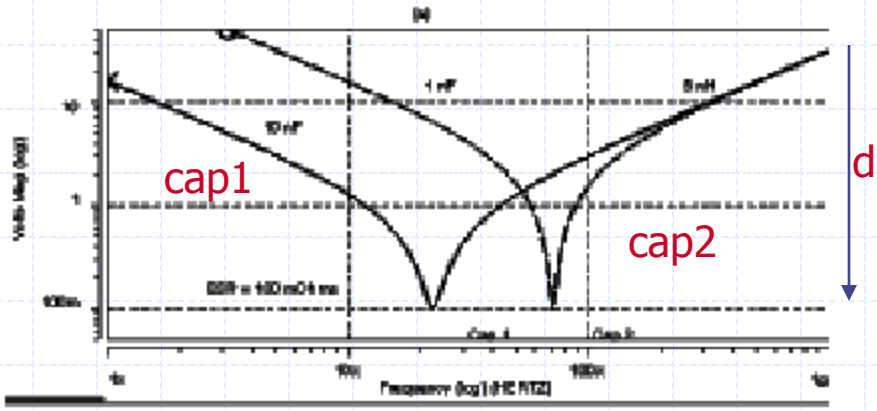


FIGURE 6.24 A simplified equivalent circuit of a capacitor including the effects of lead length showing Bode plots of the impedance: (a) magnitude; (b) phase.

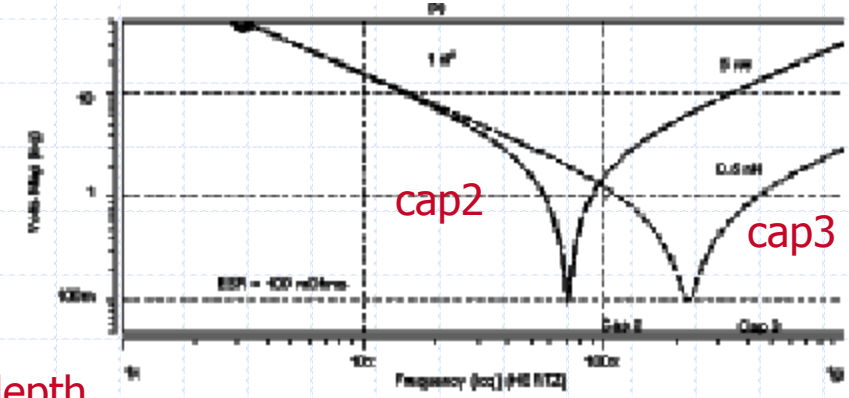
Ceramic Capacitance: Model behavior

TABLE III
CAPACITOR VALUES ANALYZED IN FIG. 6

	cap 1	cap 2	cap 3
Capicitance	10 nF	1 nF	1 nF
ESR	100 mOhm	100 mOhm	100 mOhm
Inductance	5 nH	5 nH	0.5 nH

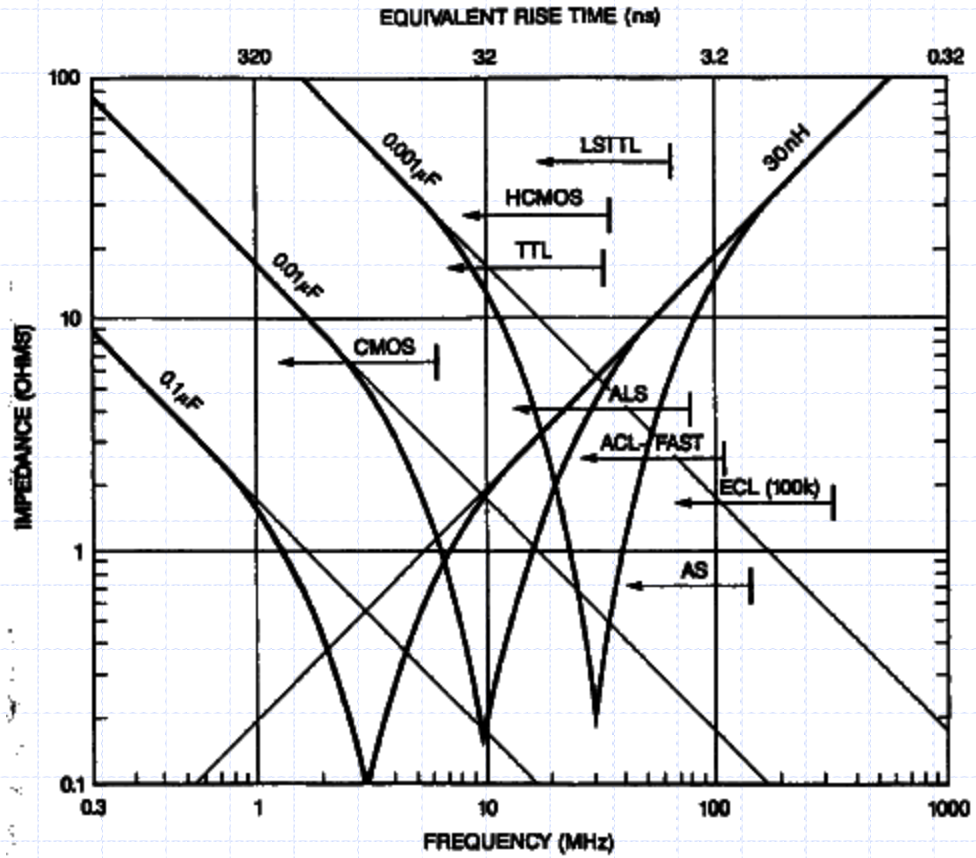


depth



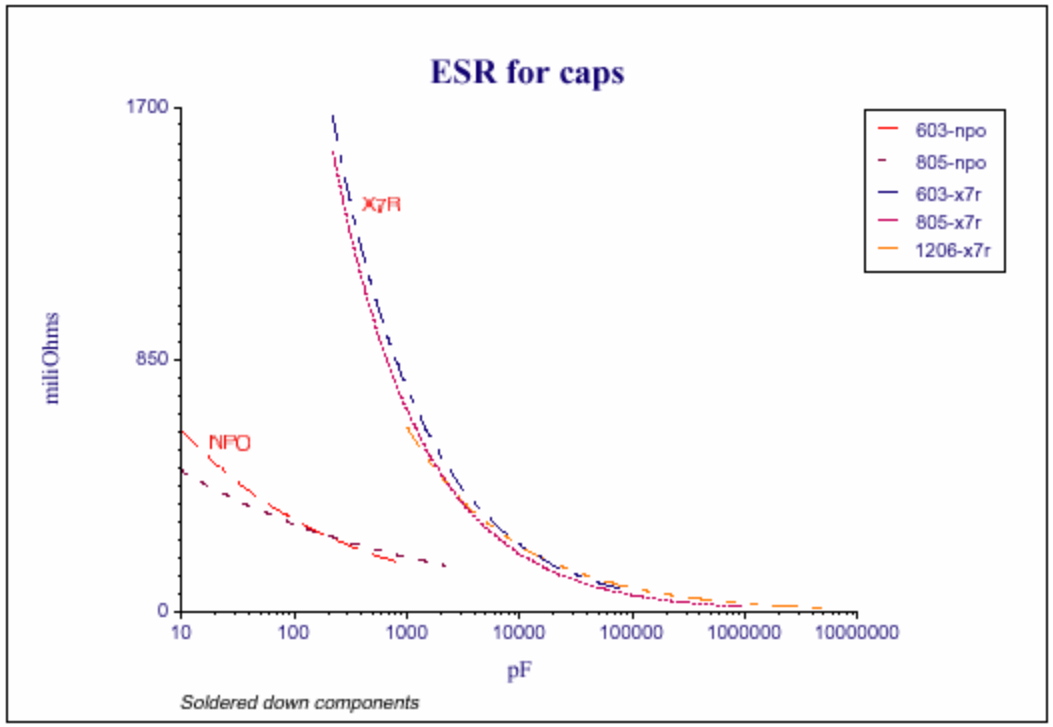
The depth is decided by what ?
The resonance frequency is decided by what ?

Ceramic Capacitance: Model behavior



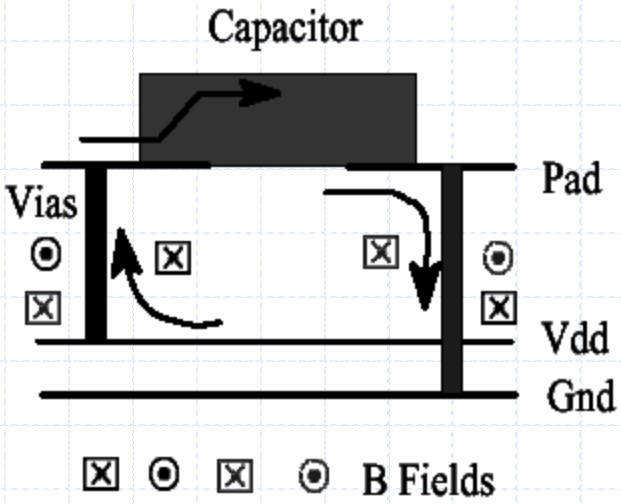
ESR of Ceramic Capacitance

ESR can be measured by the HP4291A (Impedance Analyzer) by a SMA testing fixture
A better technique employing the low impedance head connected to the IA.



ESL of Ceramic Capacitance

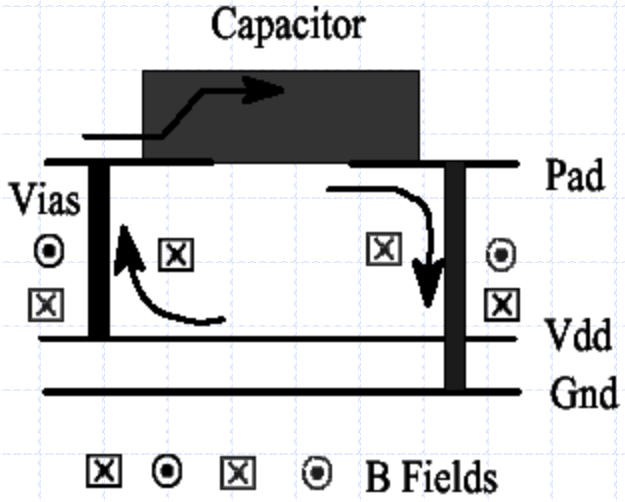
Who contributes the ESL of the decoupling capacitor ??



ESL of Ceramic Capacitance

There are THREE components of the ESL.

1. Pad layout
2. Capacitor height
3. Power plane spreading inductance

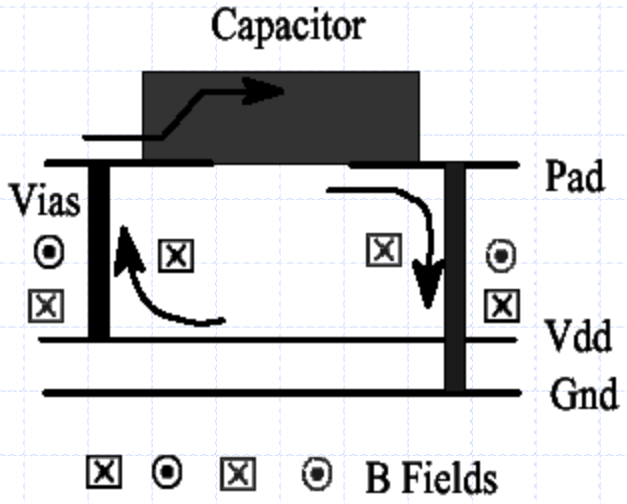


ESL of Ceramic Capacitance : Pad inductance

The pad layout consists of

1. Via placement with respect to the pad
2. The length and width of the traces connected to the pad
3. The way the via is connected to the power/ground planes

Which parts dominate the ESL of the pad layout ??



ESL of Ceramic Capacitance : Pad inductance

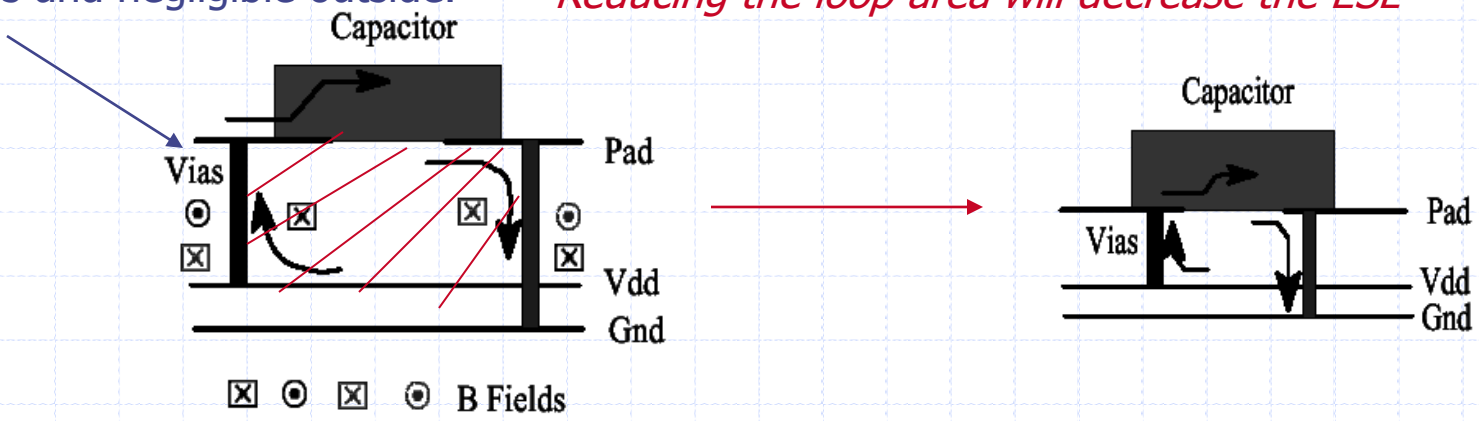
$$L \triangleq \frac{\varphi}{I}$$

$$\varphi = \oint \vec{B} \cdot d\vec{s}$$

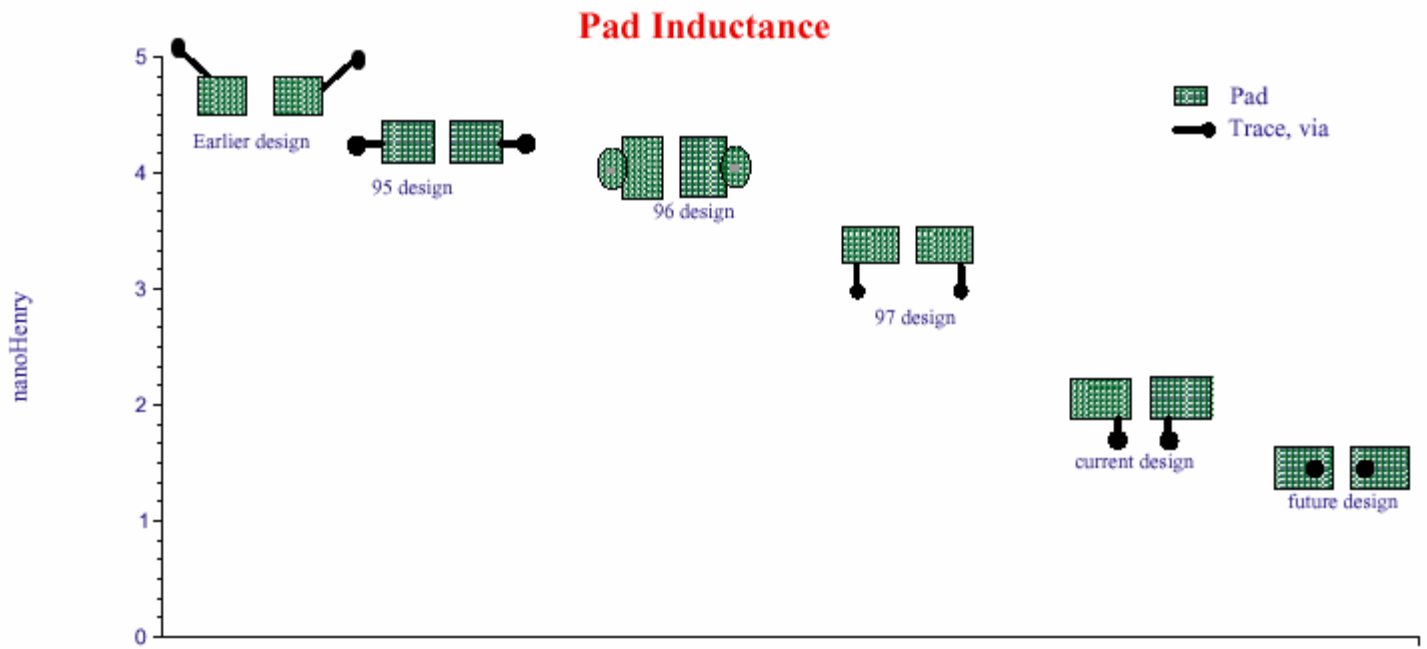
The location of the power/ground in the PCB stackup controls the height of the via which is the *major contributor* of the pad inductance.

Magnetic field concentrate between two vias and negligible outside.

Reducing the loop area will decrease the ESL

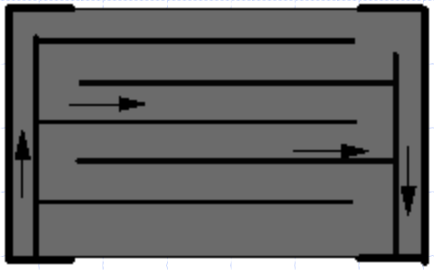


ESL of Ceramic Capacitance : Pad inductance



ESL of Ceramic Capacitance : Capacitance height

Capacitor height



For thicker capacitor, the current has to flow up and down and effectively increase the length of the current loop.

Thickness(mils)	Inductance(pH)
20	300
30	450
40	600
50	700

← 0805

Figure 10: Height adds inductance to the capacitor.

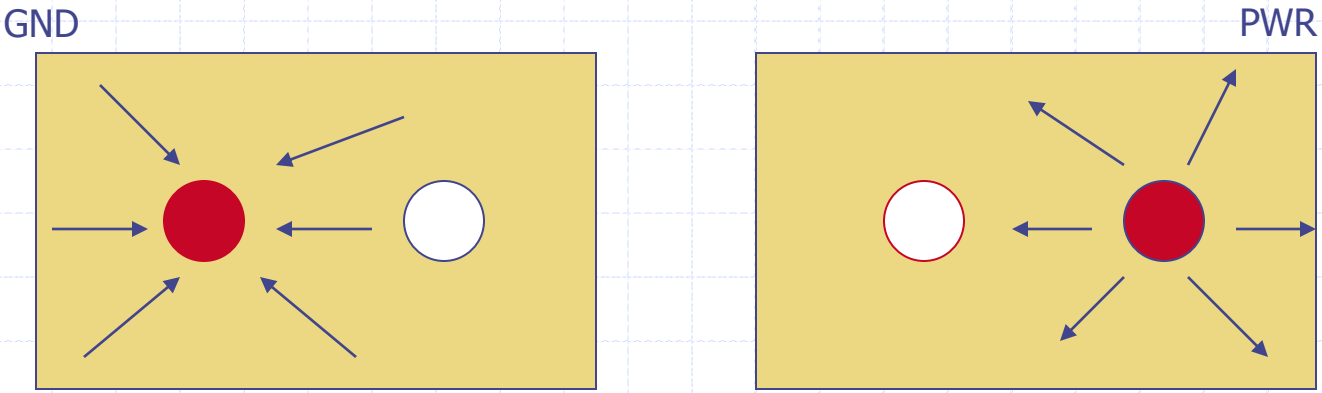
ESL of Ceramic Capacitance : PWR/GND spreading inductance

The last factor contributing to the ESL is the Spreading inductance between the PWR/GND.

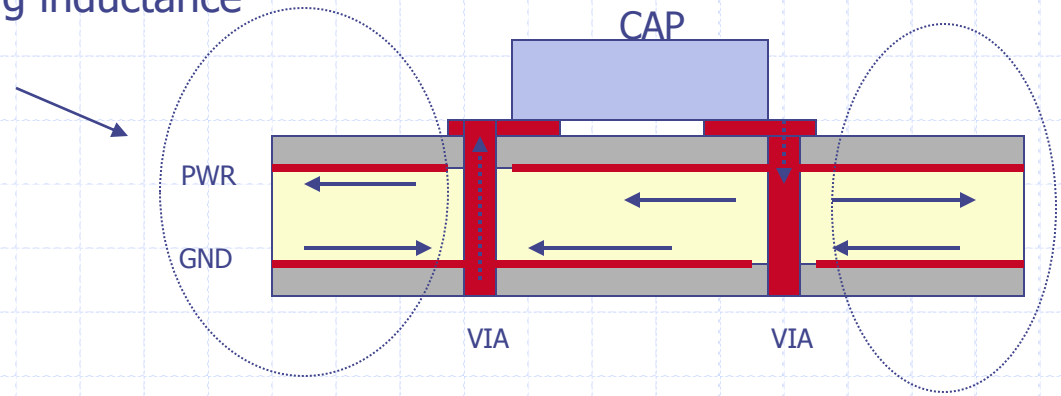
What is the meaning of the spreading inductance ?

ESL of Ceramic Capacitance : PWR/GND spreading inductance

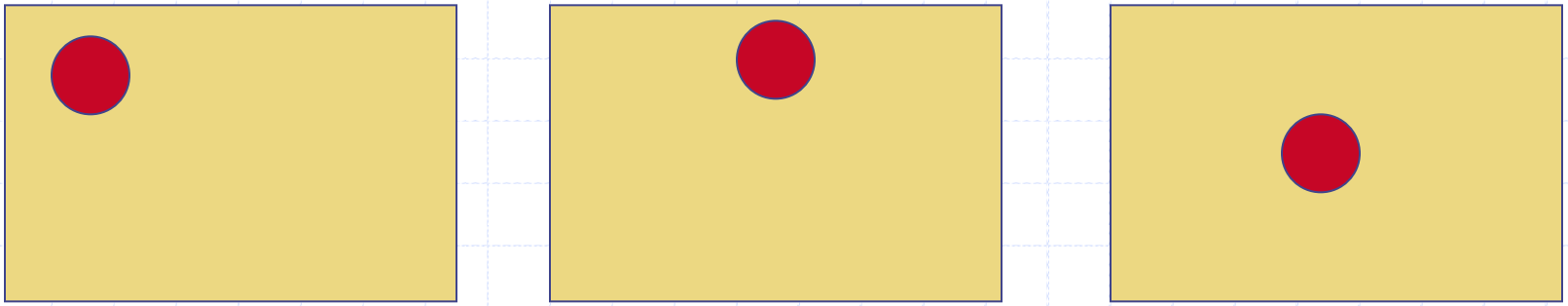
What is the meaning of the spreading inductance ?



spreading inductance



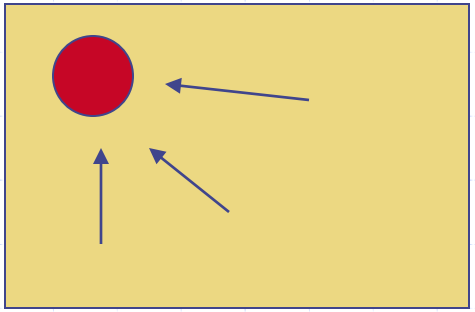
ESL of Ceramic Capacitance : PWR/GND spreading inductance



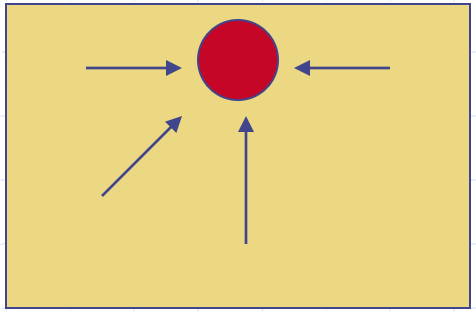
corner edge center

Which one has larger spreading inductance ? Why ?

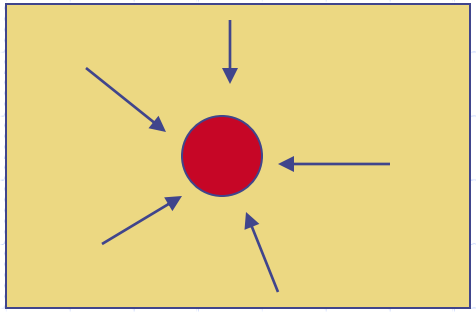
ESL of Ceramic Capacitance : PWR/GND spreading inductance



Corner 1.



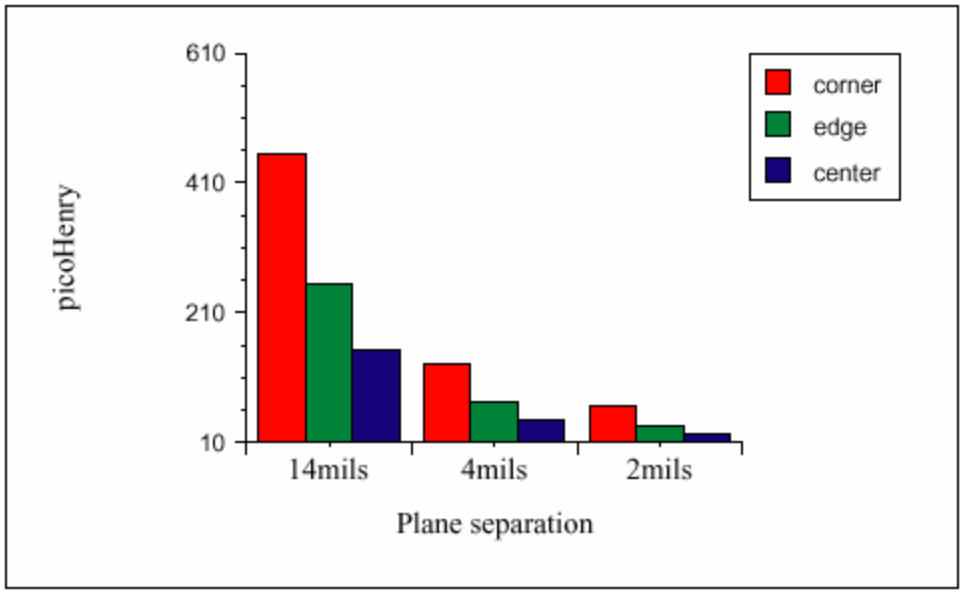
Edge 2.



Center 3.

ESL of Ceramic Capacitance : PWR/GND spreading inductance

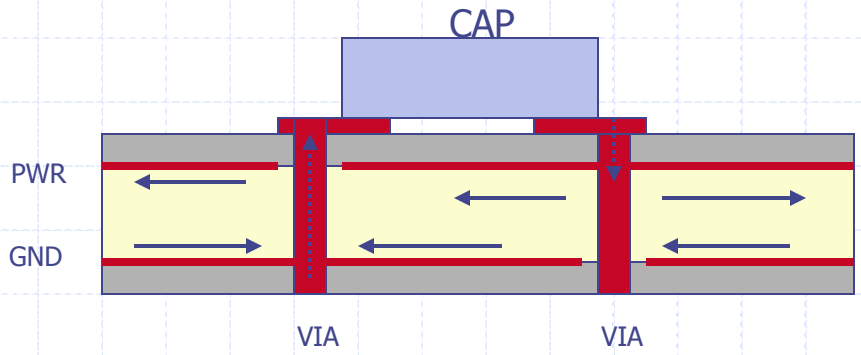
Spreading inductance for different via locations for various plane separations



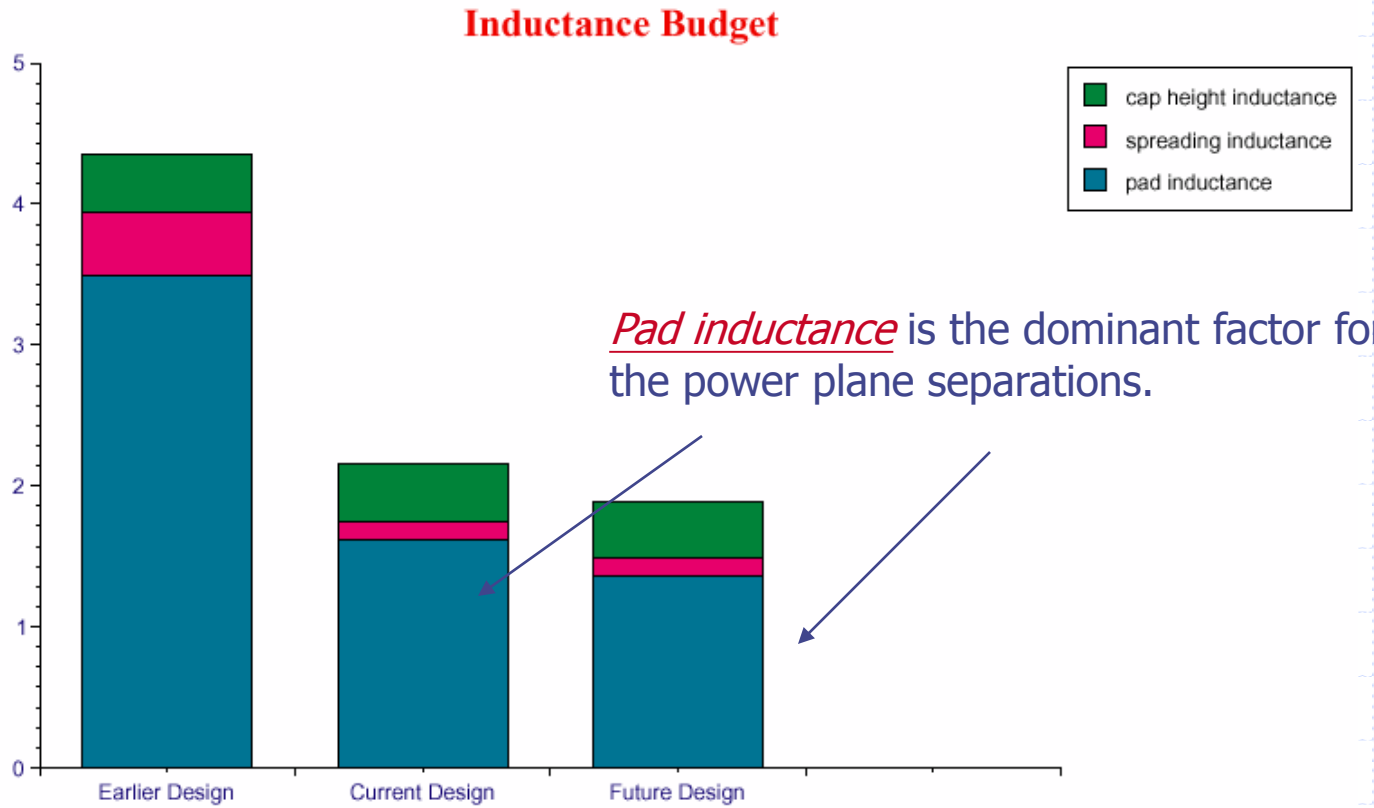
ESL of Ceramic Capacitance : Comparison

1. Pad layout
2. Capacitor height
3. Power plane spreading inductance

Which one is the main contributor of the ESL ??

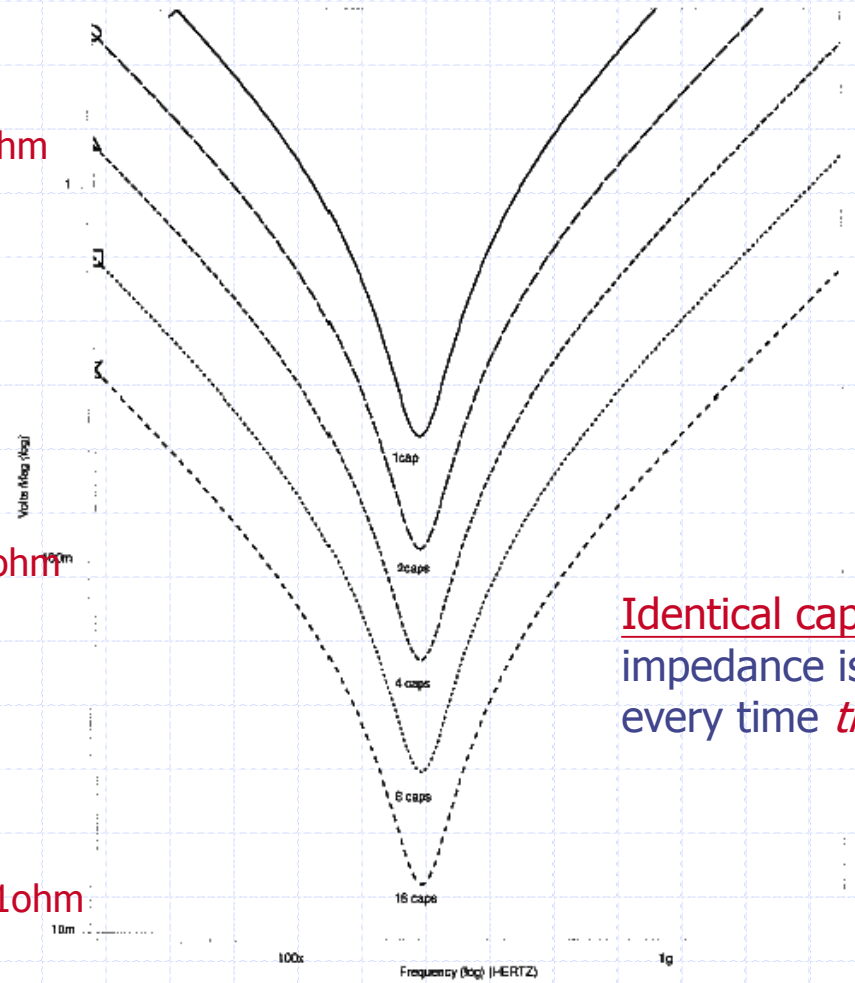


ESL of Ceramic Capacitance : Comparison



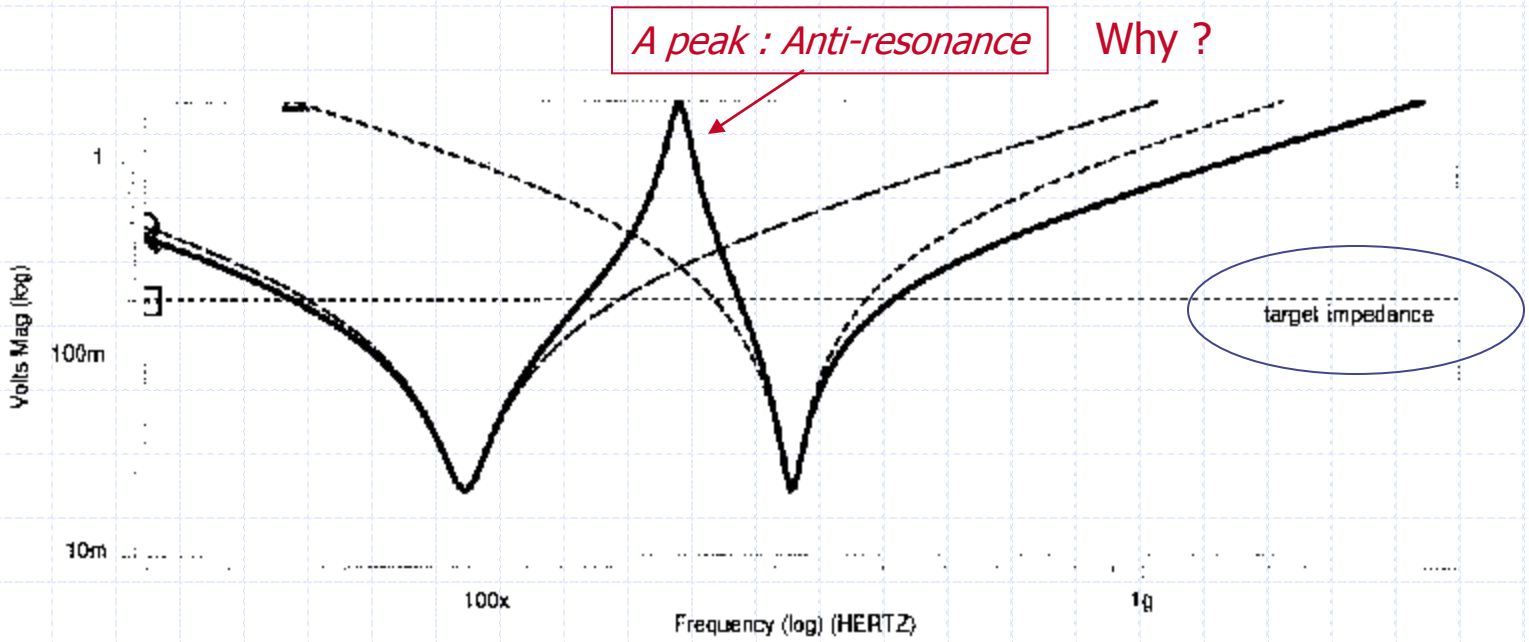
Pad inductance is the dominant factor for minimizing the power plane separations.

Shunting of Ceramic Capacitance :Identical capacitors

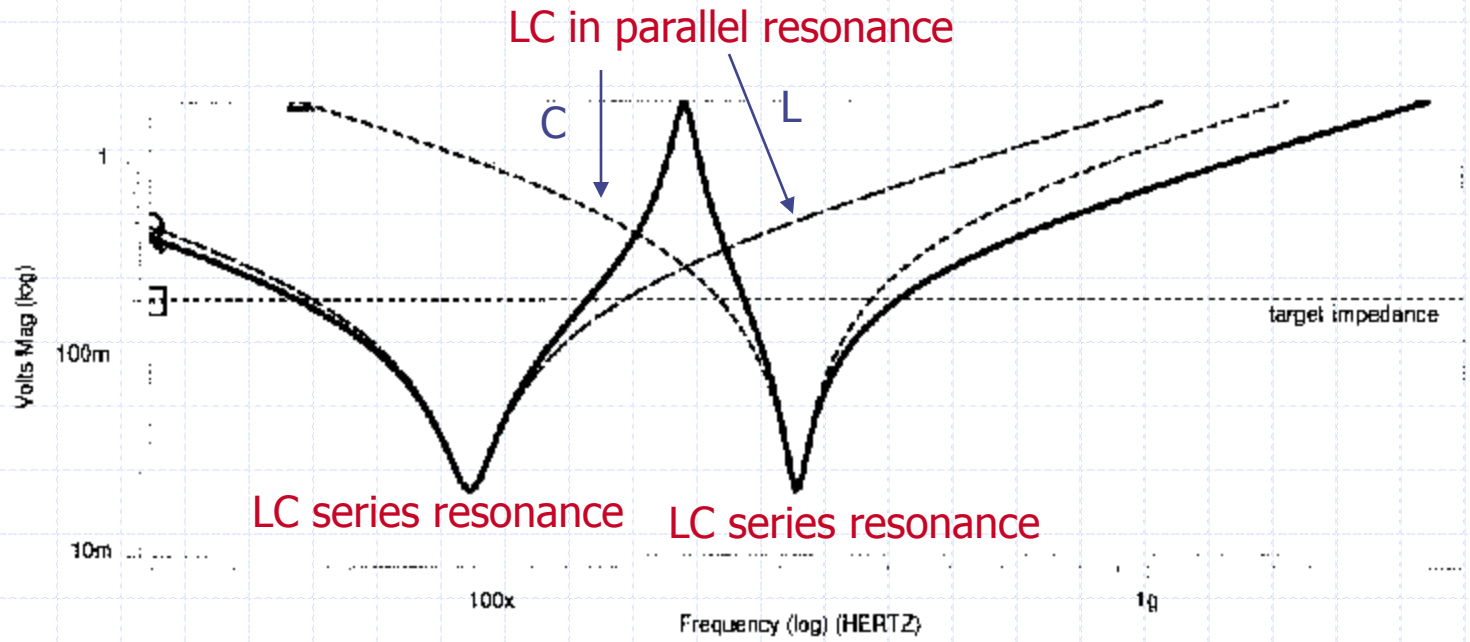


Identical capacitors in parallel. The impedance is *reduced by a factor of 2* every time *the quantity is doubled*.

Shunting of Ceramic Capacitance: different values



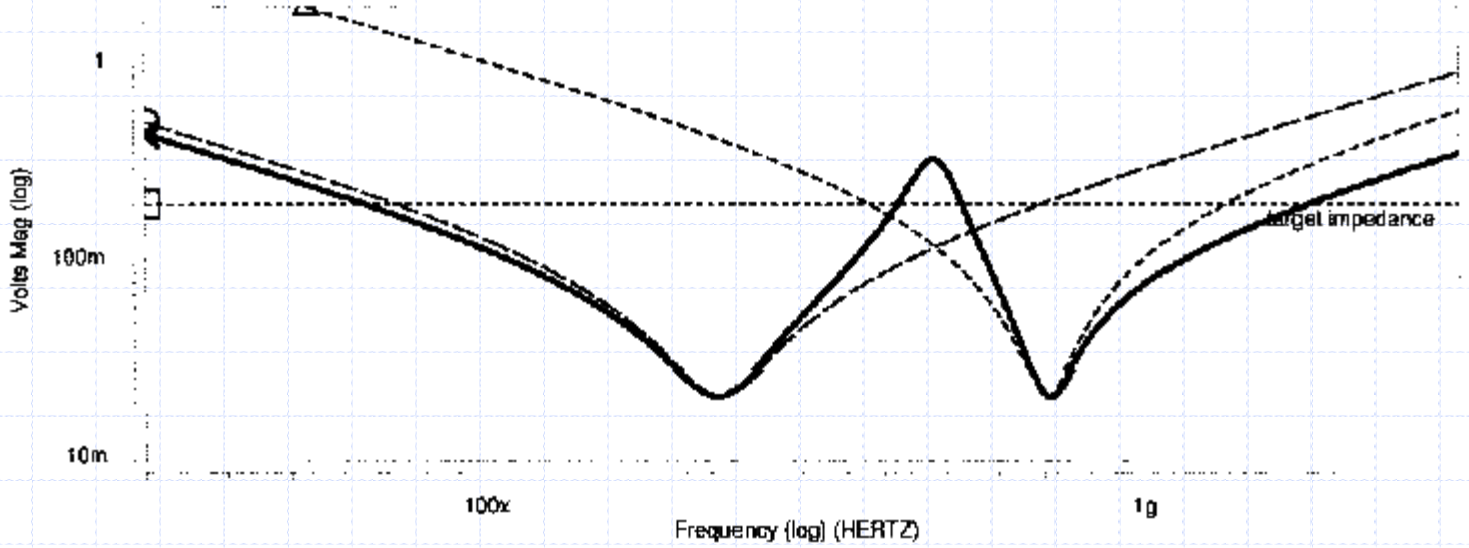
Shunting of Ceramic Capacitance: different values



How to <u>reduce</u> the peak of the anti-resonance to meet the target impedance ??

Shunting of Ceramic Capacitance: different values

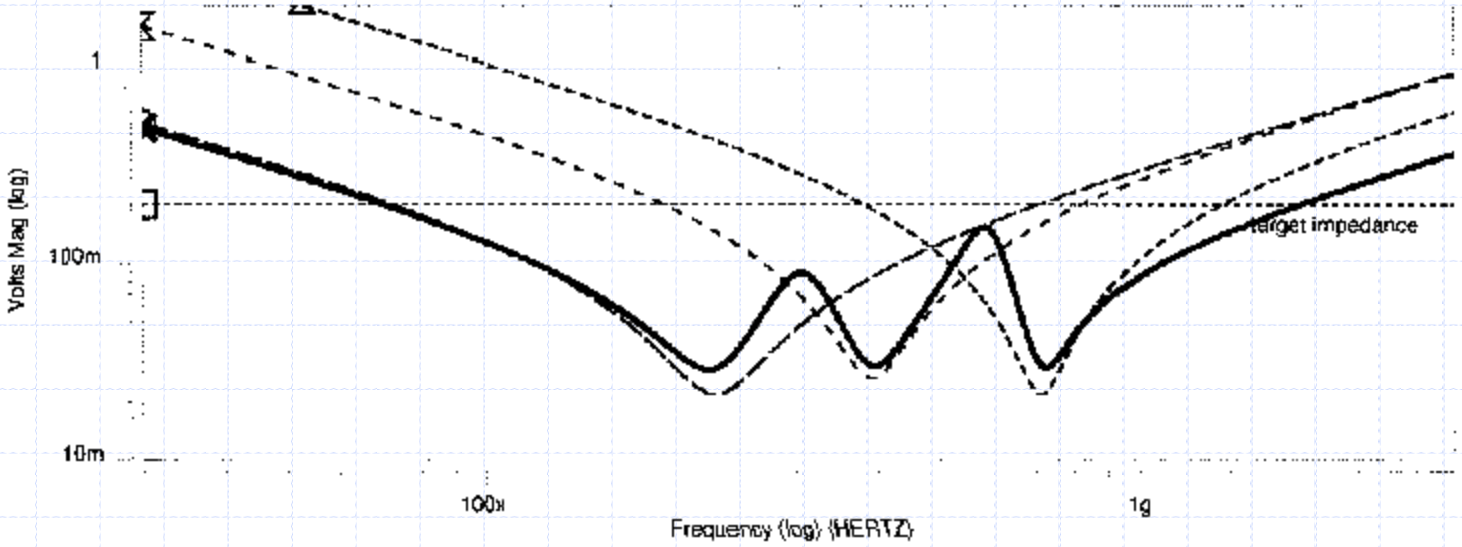
Minimizing the ESL is the most effective way to reduce the height of the peak.



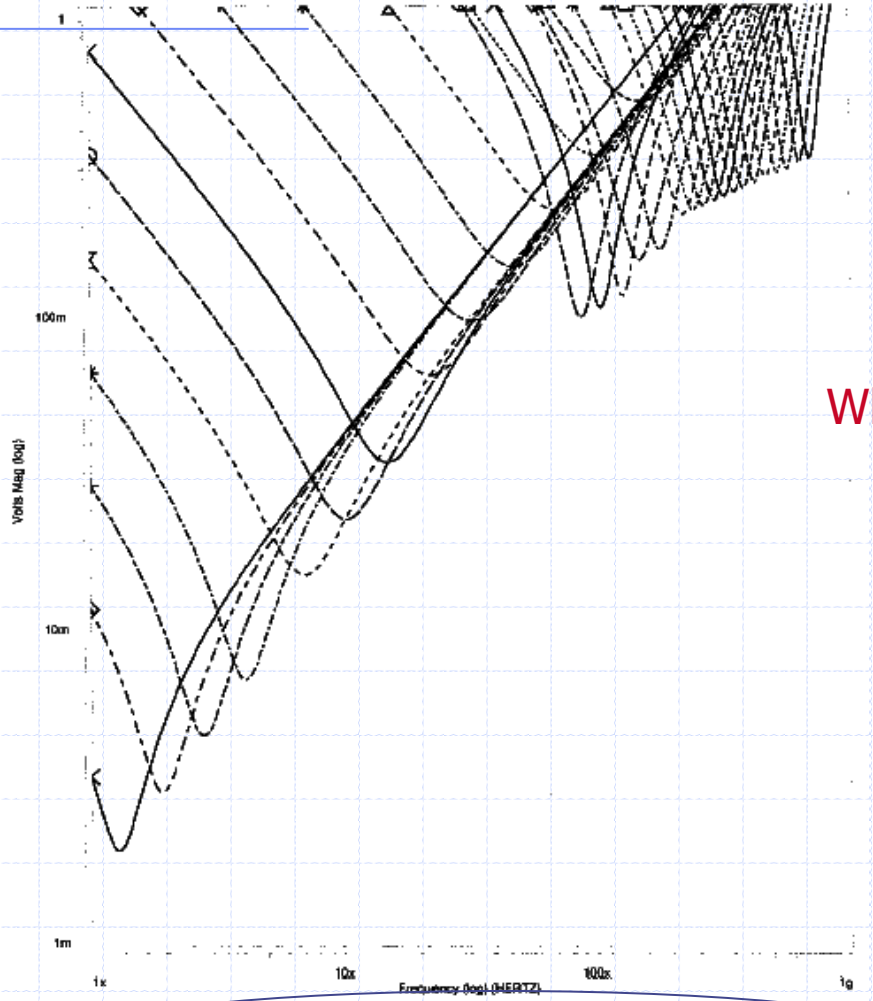
Shunting of Ceramic Capacitance: different values

The anti-resonance also becomes high if large gaps exist in capacitive value.

Three capacitors are used but with the total values being equal to the previous case.



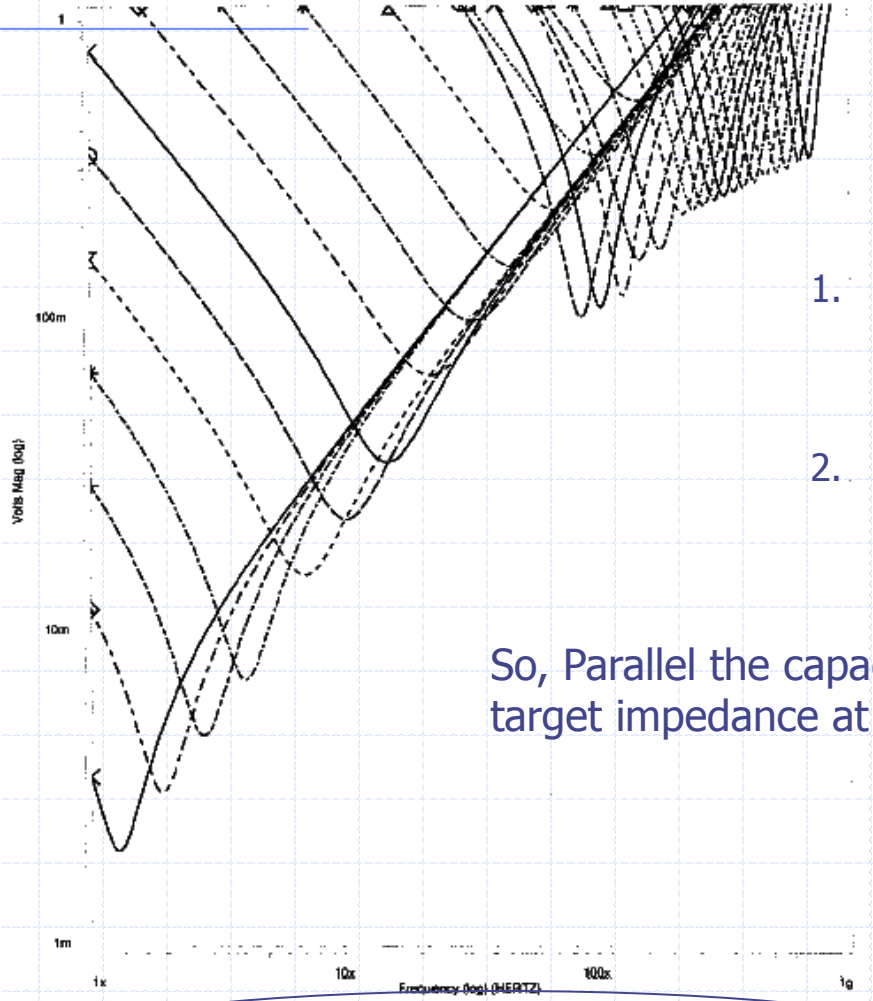
Impedance of Ceramic Capacitance



What capacitor behavior do you see ??

ig. 13. Impedance versus frequency for several X7R and NPO capacitors.

Impedance of Ceramic Capacitance



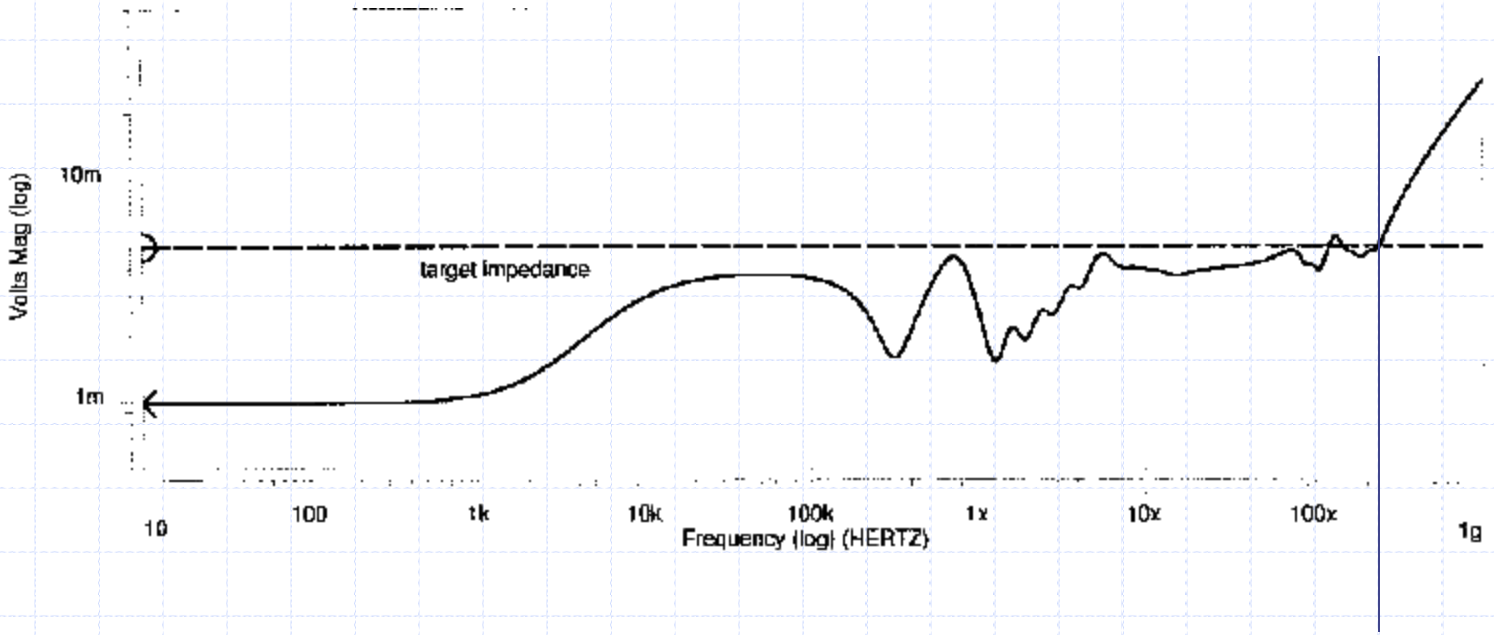
ig. 13. Impedance versus frequency for several X7R and NPO capacitors.

1. The resonance frequency goes up as the capacitance value decreases. Why? (ESL decreases)

2. The minimum impedance did not go down as the capacitance value decreases. Why? (ESR is lower for higher capacitive values)

So, Parallel the capacitor is necessary for meeting the target impedance at high frequencies.

Impedance of a complete power bus

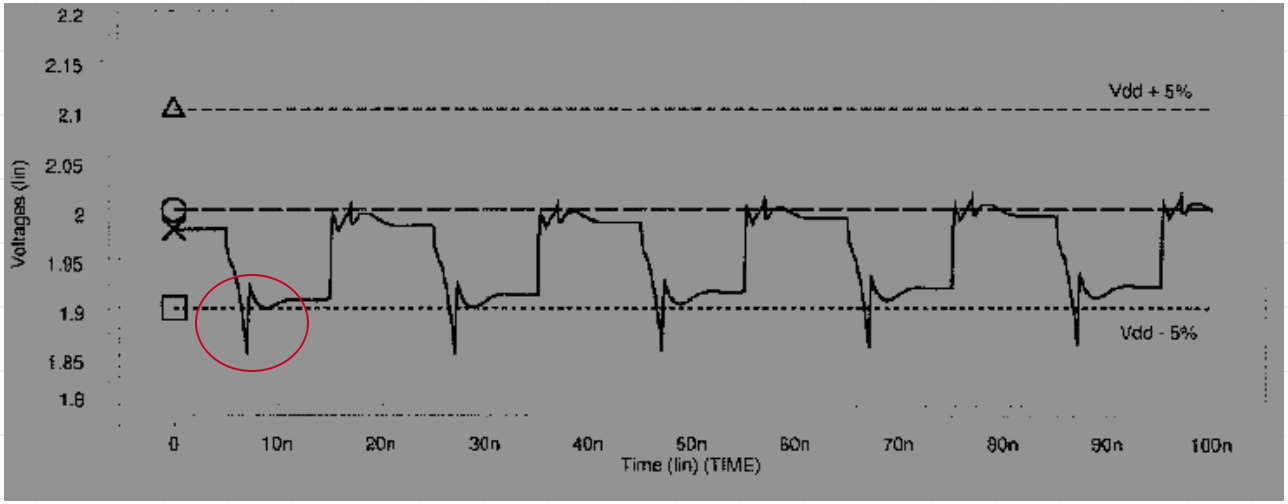


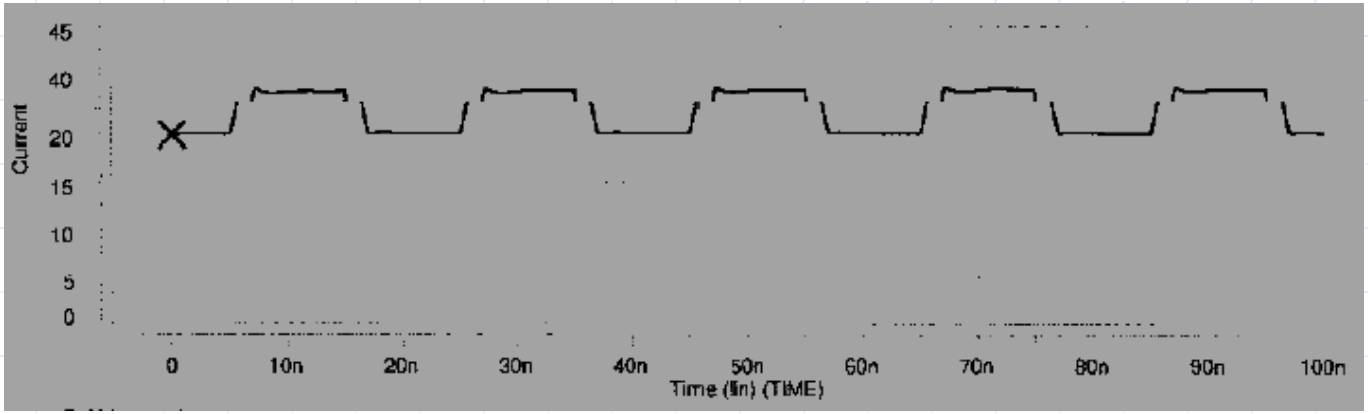
Impedance v.s. frequency of PDS with VRM, 7 bulk capacitors, 115 ceramic capacitors.

The PDS meets the target impedance up to 200MHz.

Impedance of a complete power bus

20Amp, 50MHz current transients that have 2ns rise time





Summary

The target impedance is met in the frequency domain, noise In time domain stays below a specified amount.